DANA™

Dana Laboratories Incorporated
Irvine, California 92664

Telephone (714) 833-1234
Teletype 910-595-1136

Publication

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PRELIMINARY MANUAL

Series 4400

DIGITAL MULTIMETERS

212 Module

July, 1968

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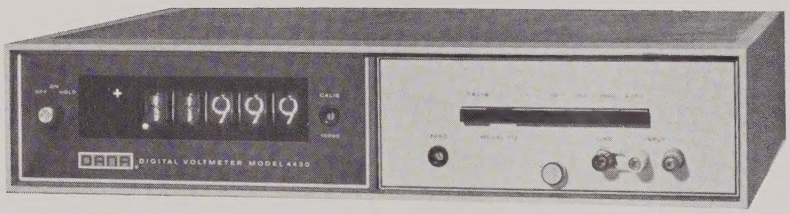


Model 4430/212

Model 4470/212

Figure 1.1. Series 4400 Digital Multimeters

SECTION 1

INTRODUCTION

1.1 INTRODUCTION

1.2. This manual describes the Dana Series 4400 Digital Multimeters (DMM). The basic models are the 4430 and the 4470 which differ only in their mechanical packaging. Model 4430 is a thin-line instrument (3-1/2 inches high) designed for standard rack mounting while Model 4470 is primarily a bench type instrument (see figure 1.1). Descriptions in this manual apply to all models unless otherwise indicated.

1.3 MECHANICAL DESCRIPTION

1.4. Each instrument consists of two modules. The Digitizing and Display Module, comprising the left-hand portion of Model 4430 and the upper half of Model 4470, contains the actual measurement circuits and is the same in all instruments in the series. The Accessory Module, comprising the right-hand side of Model 4430 and the lower half of Model 4470, contains signal conditioning circuits that provide a ten-volt full-scale (plus overrange) analog voltage for measurement by the Digitizing and Display Module.

1.5. This manual covers Accessory Module 212 which provides measurement of DC voltages on full scale ranges of .1 volt to 1000 volts. The combination of modules produce two DMM models designated as 4430-212 and 4470-212.

1.6. The power supply is common to the Accessory and Digitizing modules and is located at the rear of the instrument. The Digitizing and Display circuits are located on a single printed circuit board. The signal conditioning circuits are mounted on another single board called the Isolator. Circuits consist of integrated circuits except for critical analog circuitry where discrete components are used.

1.7. The output is displayed on a four-digit visual display with a fifth overrange digit that extends full-scale of each range by 20% (9999 to 11999). Automatic ranging is performed by internal circuits that determine the optimum range and switch to that range automatically.

1.8 ELECTRICAL DESCRIPTION

1.9. A block diagram of the DMM is shown in figure 1.2. For DC measurements, the input is applied to a voltage divider at the input that divides the input voltage by 1 or by 100 depending on the range selected. The scaled input is applied, through an active three-pole filter, to the Isolator amplifier which delivers 10 volts full-scale (12 volts, with overrange) to the Digitizing and Display module. The gain of the amplifier is either 1, 10, or 100 depending on the range.

(Paragraph 1.10 deleted)

1.11. The Digitizing and Display module measures the analog voltage from the Accessory Module by

the high-accuracy ramp technique. The amplitude of the input signal is measured by comparing it to an internally referenced integrated step function or ramp. The DMM readout displays the position of a counter that measures the time required for the ramp voltage to reach the level of the input signal. The value displayed is equal to the voltage level of the input. Readings are taken four times a second with the OFF-ON-HOLD switch in the ON position. The HOLD position permits the instrument to remain at the last reading indefinitely. Reading accuracy of the DMM is maintained through the use of a crystal-controlled counter and a highly stable, zener-regulated, internal reference voltage.

1.12 SPECIFICATIONS

1.13. Specifications are listed in table 1.1.

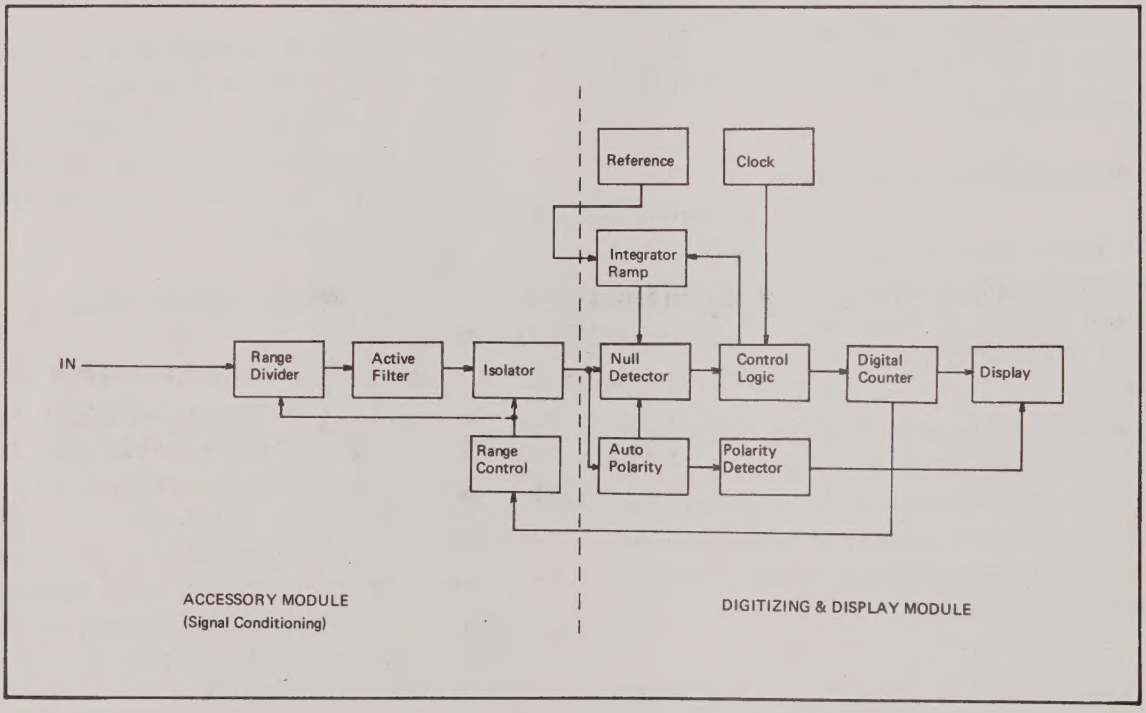


Figure 1.2. Block Diagram - 4400 Series DMM

Table 1.1
Specifications

DC VOLTS:	*Ranges (auto ranging & auto polarity):*	±.12, 1.2, 12, 120, 1200 V (1000 V MAX)
	Absolute Accuracy:	±0.01% of reading ±0.01% of F.S.
	Resolution:	10 µV
	Noise Rejection (superimposed):	60 dB, 59 Hz and up; increasing 18 dB/octave to 80 dB minimum up to 10 kHz; 50 db minimum from 10 kHz to 100 kHz; 5 volts peak-to-peak (max.) 10 kHz and above
	Common Mode Rejection:	100 dB, DC to 61 Hz, with up to 1 kilohm in either lead
	Input Resistance:	1000 megohms: 10 V range 100 megohms: 1 V range 10 megohms: 100, 1000 V ranges
GENERAL:	*Settling Time:*	0.5 second, dc mode; 2 seconds ac mode
	Maximum Common Mode Voltage:	250 volts
	Measurement Rate:	4 per second
	Warm Up Time:	1/2 hour to full accuracy
	Operating Temperature Range:	+15°C to +40°C
	Power Requirement:	15 watts, 105 to 125 V (export 210 to 250 V), 50 to 400 Hz
	Rack-mounting Hardware:	Half-rack flanges (for Model 4470), Part No. 402660 Full-rack flanges (for Model 4430), Part No. 402588
	Input Connector:	Front standard; parallel rear optional (add -1 to model number)
	Weight:	15 pounds (approx) net, 30 pounds (approx) shipping
	Dimensions:	Model 4430, 17 x 3½ x 14 inches; Model 4470, 8½ x 7 x 14 inches

SECTION 2

INSTALLATION

2.1 UNPACKING AND INSPECTION

2.2. The 4400 series DMM is sandwiched between two forms of plastic foam and packed in a double-walled cardboard carton for shipment. The plastic forms hold the DMM securely in the carton and absorb any reasonable external shock normally encountered in transit. Prior to unpacking, examine the exterior of the shipping carton for any signs of damage. Carefully remove the DMM from the carton and inspect the exterior of the instrument for any signs of damage. If damage is found, notify the carrier immediately.

2.3. The 4400 series DMM, as shipped, is designed for bench-top operation. A standup bracket is provided under the case to aid in reading the visual display. The Model 4430 instrument can be adapted for rack installation with two flange mounting holes located in each of the two side panels. The rack-mounting kit (Dana 402588) is attached to the instrument by removing and discarding the four set screws occupying the mounting screw holes and securing the two rack mounting flanges to the side panels of the instrument with the four screws contained in the rack mounting kit.

2.4. The Model 4470 can be ordered from the factory as a half-rack instrument or the standard instrument can be returned to the factory for modification to accommodate the half-rack mounting hardware.

2.5 POWER CONNECTIONS

2.6. A standard eight-foot, three-wire, power cable is supplied with the instrument. This cord connects to a three-pin power connector at the rear of the unit.

2.7 INPUT CONNECTIONS

2.8. Signal input binding posts are located on the front of the accessory module. Connections to these terminals are made with standard "banana" plugs. Make connections as described under "Manual Operation", paragraph 3.2. Instruments designated by a "dash 1" (−1) following the model number are equipped with a duplicate set of input binding posts on the rear panel of the instrument.

2.9 INITIAL CHECKOUT PROCEDURES

2.10. The following procedure is performed to verify that no damage has occurred during shipment and that the instrument is operative. Slight deviations in readings during the following tests may be corrected by making simple adjustments. For instructions refer to Section 5, "Calibration". Any major discrepancies should be reported to the carrier and to Dana Laboratories immediately.

2.11. Prior to performing the checkout procedure, it may be advisable to refer to the operating instructions beginning with paragraph 3.2. Allow one-half hour for instrument to warm up before proceeding.

2.12 ZERO CHECK

(a) Select DC and .1 range.

(b) Short input leads. Visual readout should display .00000.

(c) If necessary, adjust ZERO control on front panel to obtain this reading.

2.13 POLARITY GAIN CHECK

(a) Select DC and 10 range.

(b) Apply a known voltage of approximately -10 volts to the input. Visual readout should display value of input voltage (within specified tolerance) and proper polarity.

2.14 RANGE CHECK

(a) Select DC and 100 range.

(b) Connect input to a source of +100 volts DC.

(c) Visual readout should display input value (within specified tolerance) and proper polarity.

(d) Vary input voltage and polarity; check for proper readout.

(e) Repeat the above four steps on 1000-volt range.

(f) Select Auto range and repeat the above checks.

NOTE

If the DMM has been stored for a prolonged period (5 or 6 months) without use, it is recommended that it be operated with a variable transformer, such as a Variac, at one-half line voltage for about two hours before gradually applying full power. This is done to "reform" the electrolytic capacitors in the amplifier and reduce the chance of capacitor failure.

SECTION 3
OPERATION

3.1 CONTROLS

3.2 DIGITIZING AND DISPLAY MODULE

(Paragraphs 3.8 and 3.9 deleted)

3.3. OFF-ON-HOLD SWITCH. This dual-purpose switch applies power to the instrument and allows the selection of HOLD.

(a) OFF - all power is removed from the instrument.

(b) ON - the instrument is operating and taking readings at four per second.

(c) HOLD - "freezes" the last reading of the instrument until it is switched back to the ON position.

3.4. CALIBRATE ADJUSTMENT. This is a flat-blade screwdriver-adjusted potentiometer used in conjunction with the accessory module to calibrate this DMM. Instructions for this operation are described in paragraph 3.7.

3.5. ACCESSORY MODULE

3.6. All controls on the Model 212 Module, with the exception of the screwdriver-adjusted ZERO control, are pushbutton switches, located on the front panel.

3.7. CALIBRATE SWITCH. This is a momentary switch that causes a test reading to appear in the DMM display readout as long as the switch is depressed. The DMM is calibrated by adjusting the calibration potentiometer on the DMM for a readout of -.10000 (decimal shown for .1V range).

3.10. RANGE CONTROL. The range control consists of six interlocking pushbutton switches: .1, 1, 10, 100, 1000 and AUTO.

(a) Manual ranges. Ranges are selected by depressing the appropriate switch. The switches are interlocked so that as one range switch is depressed, the previously selected range switch is returned to open position.

(b) Auto range. This mode allows the DVM to select the range that provides the highest accuracy for the signal being measured. This switch is interlocked with the four range switches.

3.11. ZERO ADJUST. To zero the DMM, short the two input leads together, select DC and autorange. Adjust the ZERO potentiometer for a DMM readout display of 00000.

3.12 OPERATION

3.13. GENERAL. The instrument has been designed for the simplest possible level of operation. Once the instrument has been connected to the power line and to the signal source in accordance with the instructions, the operator can make all the required measurements by setting the front

panel controls to the indicated positions.

> CAUTION
>
> Voltage applied between ground and the low-input terminal must not exceed 250 volts.

3.14. DC MEASUREMENTS. Attach the high side of the signal source to the red signal input terminal, the low side to the white signal input terminal. Normally, the ground terminal (which is at the DMM Chassis Ground) is jumpered to the white signal input terminal by the supplied shorting bar. To operate the DMM on a floating basis, detach the ground terminal from the white input terminal.

(Paragraph 3.15 deleted)

SECTION 4

THEORY OF OPERATION

4.1 INTRODUCTION

4.2. Theory of operation of the 4400 Series DMM is described in two parts. First, the Accessory (signal conditioning) Module is described; then the Digitizing and Display Module. The purpose of the Accessory Module is to supply a 10-volt analog voltage for measurement in the Digitizing and Display Module.

4.3. Diagrams used in this section are intended to supplement the complete schematics included in Section 6. All logic circuits are defined at the end of this section.

4.4 ACCESSORY MODULE

4.5. Accessory Module 212 provides a ten-volt full scale (12 volts with overrange) analog signal for measurement by the Digitizing and Display Module. The circuits are mounted on a single Isolator Board. This board contains the isolator amplifier, range control circuits, and an active filter.

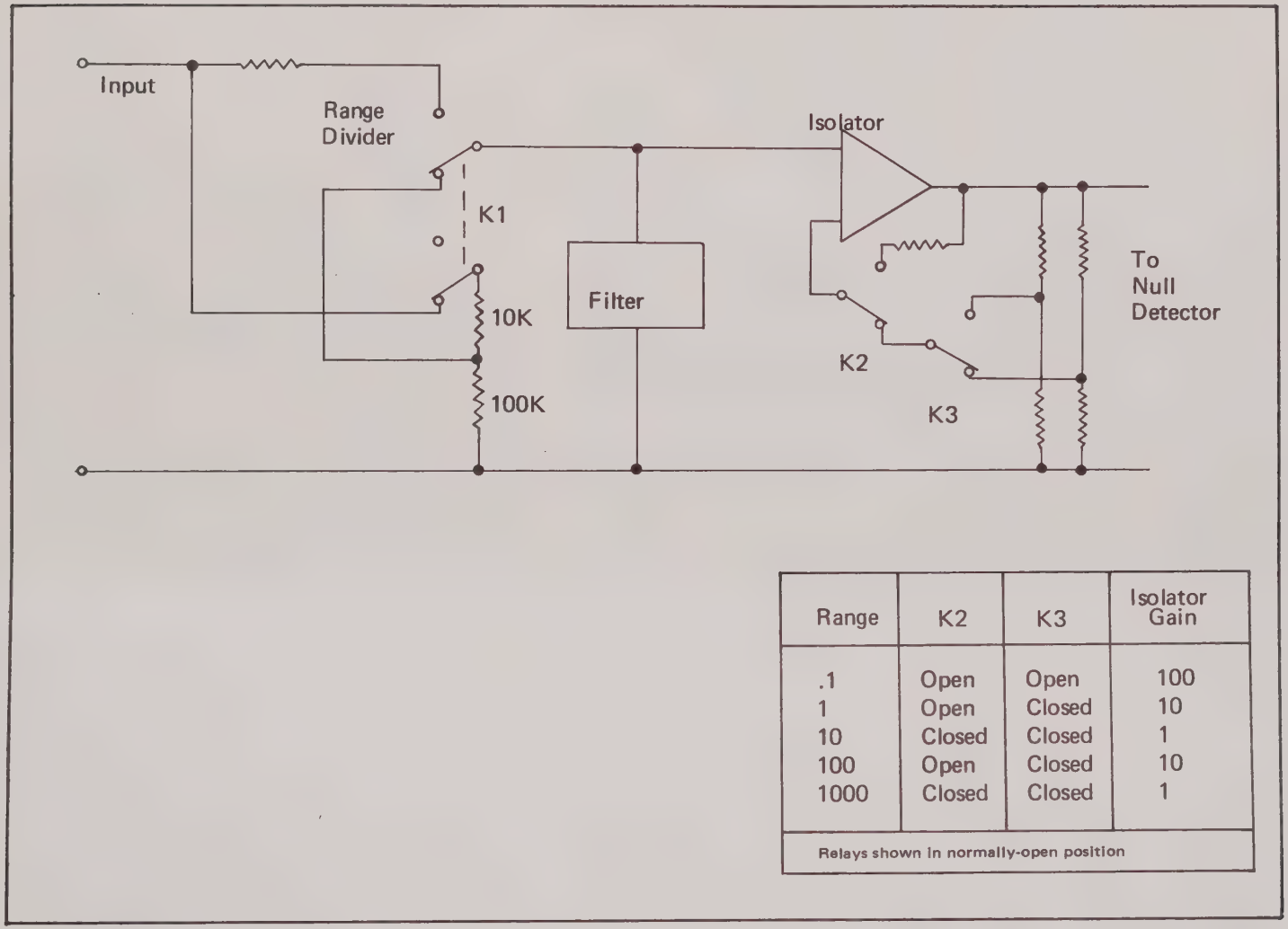
4.6 ISOLATOR (Figure 4.1)

4.7. The Isolator is a floating input potentiometric amplifier capable of operating at very low signal levels. Its output is a 10-volt full scale analog voltage (12 volts, in overrange) that is applied to the Digitizing module for measurement. The amplifier operates at a gain of one, ten, or a gain of one hundred, depending on the range (see Table 4.1). The gain is switched by relays K2 and K3 that control a resistor divider into the feedback circuit when energized.

4.8. The input to the Isolator is applied through a ranging network that divides the input by 1 or by

Table 4.1. Range Logic

Range	Logic	F/S Isolator Input	Isolator Gain	Relay Position		
				K1	K2	K3
0.1V	R1 R2 R3	.1V	100	Open	Open	Open
1V	$\overline{R1}$ $\overline{R2}$ $\overline{R3}$	1V	10	Open	Open	Closed
10V	R1 $\overline{R2}$ $\overline{R3}$	10V	1	Open	Closed	Closed
100V	$\overline{R1}$ R2 $\overline{R3}$	1V	10	Closed	Open	Closed
1000V	R1 R2 $\overline{R3}$	10V	1	Closed	Closed	Closed



Range	K2	K3	Isolator Gain
.1	Open	Open	100
1	Open	Closed	10
10	Closed	Closed	1
100	Open	Closed	10
1000	Closed	Closed	1

Relays shown in normally-open position

Figure 4.1. Simplified Diagram - Accessory Module

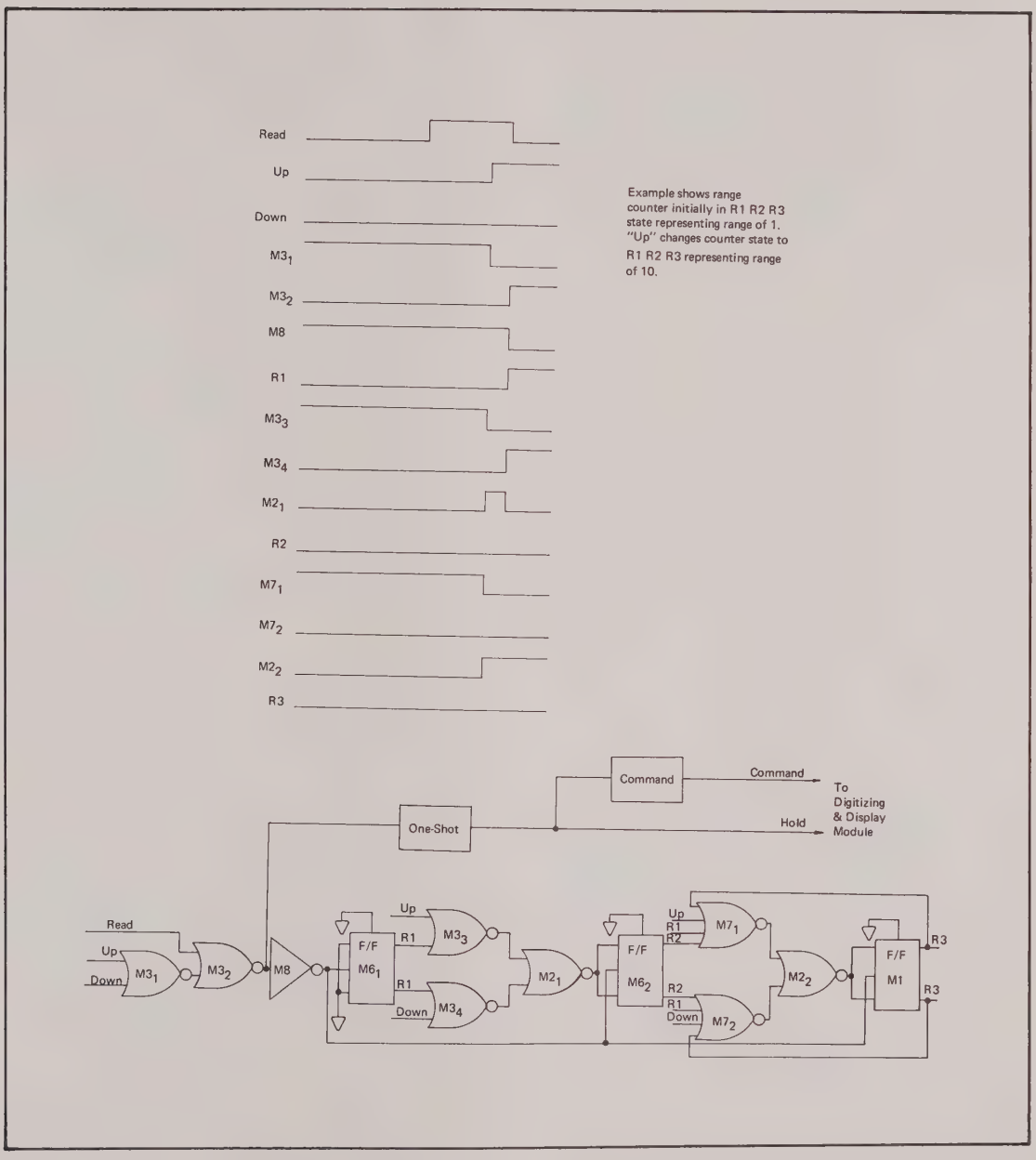


Figure 4.2. Range Control

100, depending on the state of relay K1. This relay and relays K2 and K3 are operated by the range control signals R1, R2, R3 and their complements. Operation of the relays is such that the voltage divider at the input and Isolator gain combine to deliver 10 volts full scale in all measurement modes.

(Paragraphs 4.9 through 4.12 deleted)

4.13 RANGE CONTROL (Figure 4.2)

4.14. Ranging of the instrument is controlled by a three stage flip-flop counter driven by control signals from the Digitizing and Display Module. These Control Signals are Up Range, Down Range and Read.

4.15. Up Range is true when the instrument is not on the highest range (1000) and the counter is 12000. Down Range is true when the instrument is not on the lowest range (1) and the counter is 00999 or less. Read is true during the measurement period (in the Digitizing and Display Module) of 13 ms. The negative-going edge of this signal indicates the end of the measurement.

4.16. The counter counts up or down in response to the Up Range and Down Range control signals. The state of the flip-flops corresponds to the codes and ranges listed in table 1. A manually-selected range "forces" the flip-flops to the proper state by clamping the appropriate counter outputs to common.

4.17. A one-shot circuit provides a timeout (delay) of about 0.5 sec. at the end of a measurement period to allow time for ranging and for settling time of analog circuits. During this period, the HOLD line goes positive. This line is tied to the input of the control logic circuits in the Digitizing and Display Module where the positive level prevents a new reading from being taken.

4.18. When operating in a selected range, rather than autorange, the HOLD line is permanently strapped to common by the range switch and new readings are allowed during a range changing attempt.

4.19. At the end of the Timeout, a Read command consisting of a positive pulse is sent to the control logic circuits to command a new reading.

4.20 ACTIVE FILTER

4.21. The filter (figure 4.3) is a three-pole broadband active filter used in both AC and DC measurements. The circuit, a modified gaussian filter, provides normal mode noise rejection of 60 dB at 60 Hz increasing 18 dB per octave to 80 dB.

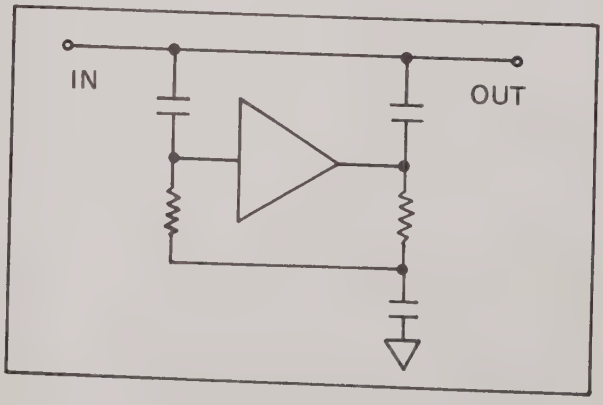


Figure 4.3. Active Filter

The DC signal from the accessory module (a) is applied to the Auto Polarity and Null Detector. This circuitry draws a precise one milliamp of current per input volt from the Null Detector summing node, regardless of the polarity of the input signal. Supplying current to the summing node is an internally referenced integrator, or ramp, which generates a positive, linearly-increasing output voltage (b). A resistor is connected from the output of the ramp to the summing node to supply the current. At the start of a read cycle, the counter is at zero (the 1mHz clock train (f) is inhibited from the counter input at gate (g) by the output of the Control Logic) and the switch across the integrating capacitor of the ramp is on, causing the output of the ramp to be at zero. When a pulse from the Read Rate logic (c) is received at the control logic, the control logic output (d) enables gate (g) and the ramp generator (b).

As the voltage output of the ramp increases, more and more current is supplied to the summing node of the Null Detector. At the same time, the counter is registering the pulses received through gate (d). At the instant the current supplied to the node by the ramp generator is equal to the current drawn from the node by the input, the Null Detector produces a pulse (e) resetting the control logic. The output of the control logic (d) goes false, stopping the counter and resetting the ramp to zero, BCD-to-decimal converters decode and transmit information from the counter to the readout tubes where the value of the DC input is visually displayed. The polarity sense circuitry monitors the output of the auto polarity amplifier and selects the polarity symbol displayed. In the event the input voltage to the Digitizing and Display portion of the DMM is greater than the instrument is able to read; the DMM follows the prescribed read cycle until the counter reaches 12,000. At this time, the 12,000 sense circuitry bypasses the Null Detector and resets the control logic. The display reads 12,000 and the overload indicator lights.

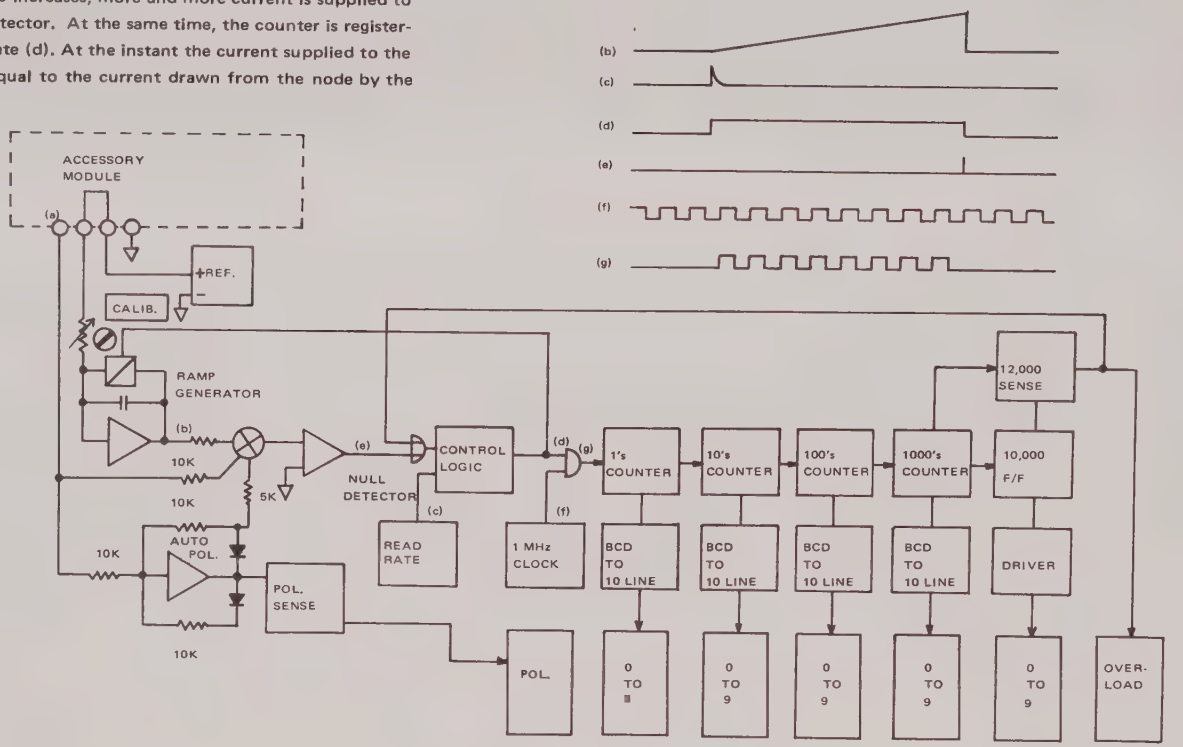


Figure 4.4. Block Diagram - Digitizing and Display Module

4.22 DIGITIZING AND DISPLAY MODULE

4.23. A simplified block diagram of the Digitizing and Display Module is shown in figure 4.4.

4.24 AUTO POLARITY

4.25. The Auto Polarity is a high gain amplifier having two polarity-selected negative feedback paths. The Auto Polarity circuitry eliminates the need for polarity switching by maintaining (in conjunction with the Accessory Module) a negative input to the Null Detector, regardless of the polarity of the input. The output of the amplifier is routed through two diodes, one allowing current to flow during a negative output through one feedback leg, and the other allowing current to flow during a positive output through the other feedback leg (see figure 4.5). The two legs, designated "-" and "+", respectively, provide negative feedback to the input of the amplifier, resulting in a closed-loop gain of minus one. The Auto Polarity amplifier network is used with the Accessory Module output to provide the negative source. The output of the accessory is routed through a 10K resistor to the summing junction of the Null Detector. The negative leg (leg conducting during a negative output of the Auto Polarity amplifier) is connected to the same summing junction through a 5K resistor. When a negative voltage output from the Accessory Module is applied to the Digitizing and Display portion of the DMM, a current is drawn from the summing junction through the 10K resistor. The output of the Auto Polarity is positive, so the "-" leg is non-conducting and has no effect on the summing junction. A positive voltage from the Accessory Module, on the other hand, feeds current into the summing junction through the 10K resistor. At the same time, an amount of current equal to twice the current flowing through the 10K resistor is being drawn from the summing junction through the 5K resistor of the non-conducting '-' leg of the Auto Polarity amplifier. The net sum is a current drain due to the positive input that is equal to the drain produced by an equal amount of voltage of the opposite polarity or negative. Therefore, the summing junction of the Null Detector sees a current drain regardless of the polarity of the input.

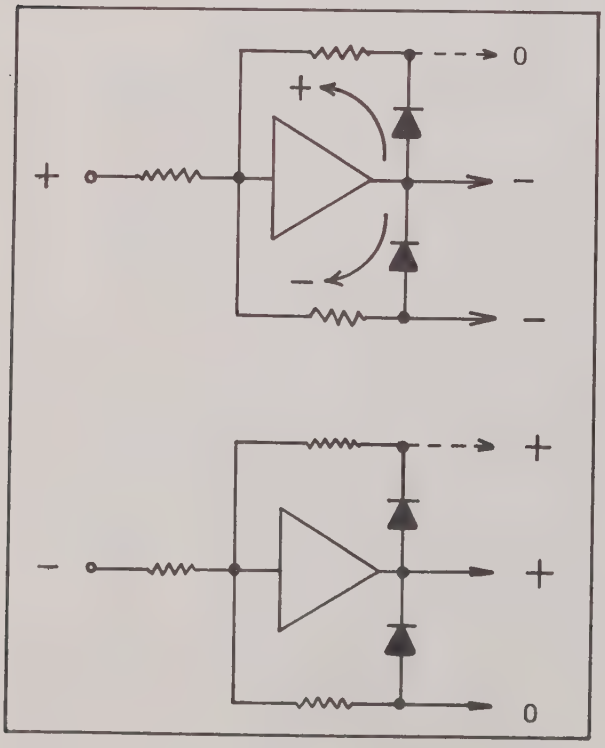


Figure 4.5. Auto Polarity Circuit

4.26 RAMP (Figure 4.6)

4.27. The ramp is an operational amplifier having a capacitive rather than a resistive feedback circuit. The result is an integrator which converts a current input to a continuous, linearly-increasing voltage output. This output, when plotted against time, forms a ramp; thus its name. Since the voltage varies directly with time, any given period of time can be equated with a certain voltage (within the limitations of this amplifier). By providing the ramp (or voltage-to-time converter) with a precise

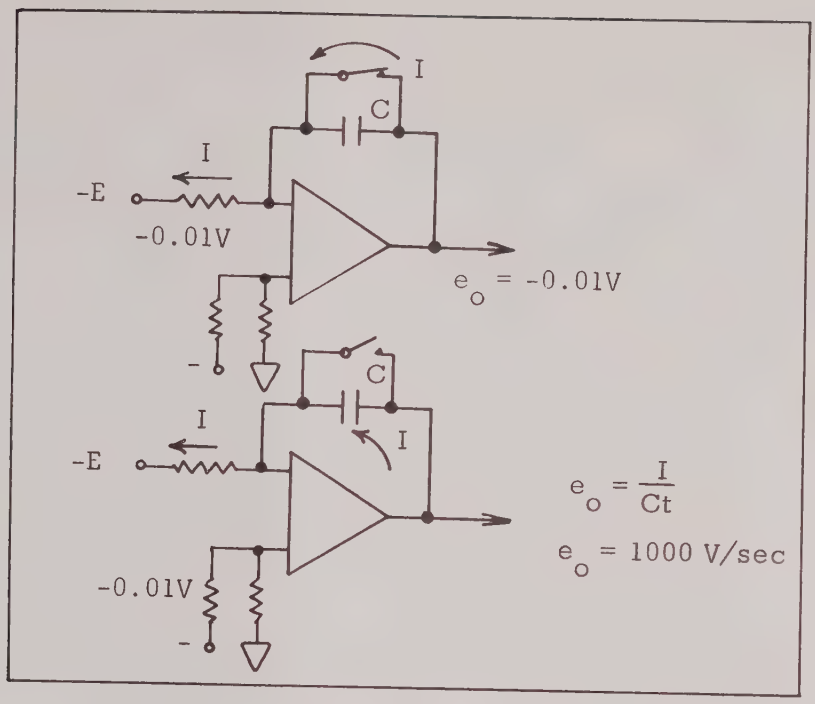


Figure 4.6. Ramp

input current, the ramp becomes a reference by which voltage measurements can be made. Prior to the initiating of a read cycle, a low-leakage switching transistor, shunting the integrating capacitor, is conducting. This causes the output of the ramp amplifier to maintain a voltage level of approximately -10 millivolts determined by a fixed voltage divider. At the start of a read cycle, the switching transistor is turned off, allowing the capacitor to charge and the ramp output voltage goes positive at a rate of one volt per millisecond. The negative bias to the input (voltage divider) allows the ramp time to settle prior to passing through zero volts.

4.28 INTERNAL REFERENCE (Figure 4.7)

4.29. The internal reference voltage is generated by a highly stable zener diode and, in conjunction with a resistor, draws a precise current from the ramp. The zener is supplied with a specific current by the four-stage reference amplifier which allows the reference to operate at its zero temperature coefficient. Because loading on the reference zener is constant, the reference voltage is taken directly from across the zener terminals, without requiring further buffering.

4.30 NULL DETECTOR (Figure 4.8)

4.31. The Null Detector is an open loop high-gain amplifier that determines when the ramp output and accessory module output are of equal potential.

4.32. Prior to a Read Command, the output of the Accessory Module, in conjunction with the output of the Auto Polarity, produces a current drain from the summing node at the input to the Null Detector. Another current drain is produced by a resistor connecting the Null Detector summing node to the output of the ramp (the output, prior to the read command, is at -10 millivolts). Upon receipt of the read cycle, the ramp output goes positive and supplies current to the summing node. When the algebraic sum of the currents equals zero, the Null Detector signals the ramp to reset and the counter to stop.

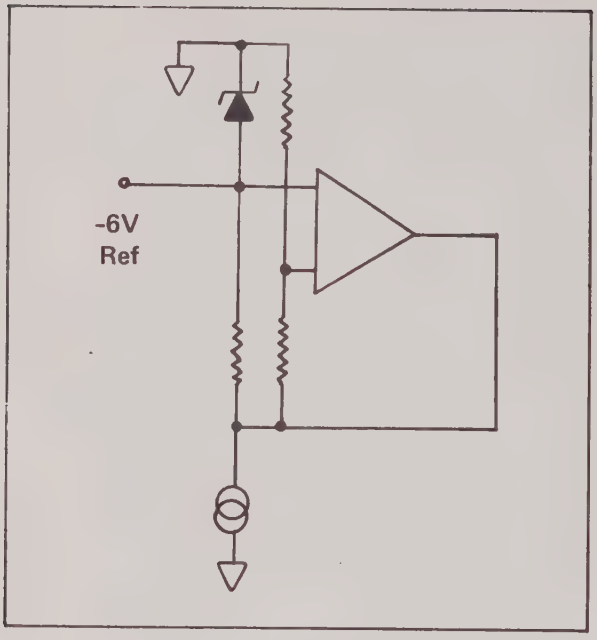


Figure 4.7. Internal Reference

4.33 BINARY COUNTER (Figure 4.9)

4.34. The counter digitally measures the time required for the ramp to reach the potential of the Accessory Module output. Prior to a read command, the counter is at zero and $\overline{Q}$ of the precount flip-flop is true, inhibiting the 10's decade. When the DMM is commanded to read, clock pulses are fed into the 1's decade, causing the decade to count. On the tenth count, a pulse appears at the input of the NOR gate feeding the 10's decade, but is blocked by the positive bias of $\overline{Q}$ of the precount flip-flop. At the same time, the precount flip-flop is reset and the counter is again at all zeros. The counter begins counting for a second time, but without the 10's decade being inhibited. The counter continues to count until stopped by the Null Detector or the overload circuitry. The first ten counts of the binary counter allow for the settling time of the ramp generator. The DMM is calibrated so that the ramp output crosses the zero volts axis at precisely the same instant that the binary counter begins its second count.

4.35 CONTROL LOGIC

4.36. The control logic covers the four logic circuits which program the various functions of the DMM.

4.37. Rate Control. This circuitry determines the number of readings taken by the DMM for a given time period (figure 4.10). Under normal reading conditions, the rate control allows the DMM to take four readings per second. During a range change, a timeout is generated and inhibits further readings until the change is complete. At completion, a read command pulse is generated, causing the DMM to take a new reading. Timing for the read rate circuit is controlled by a unijunction oscillator that produces a six-millisecond pulse every 250 milliseconds. The pulse is applied to two one-shot generators. One-shot (b) produces a 20-microsecond preset pulse. The preset pulse is used to preset the binary counter flip-flops and the precount flip-flop. The preset is also used by the range logic and a portion of the control logic. One-shot (a) produces a 13-millisecond read pulse. The leading edge of the read pulse enables the setting of the polarity indicator and initiates a range change when required (with auto range selected). The read pulse is inverted and used by the read control logic.

4.38. Read Control. The read control circuit coordinates the rate control output with the clock to properly time the start of the ramp and counter circuits. The circuit is shown in figure 4.11. Two NOR gates (c and d) are interconnected to form an R-S type flip-flop. Prior to a reading, the output of of the flip-flop is held false by the positive output of the rate control circuit. The positive level at the input of the NOR gate (a) inhibits the clock pulse from the set side of the flip-flop. At the start of a read cycle, the rate control output goes false and the 20 microsecond reset pulse goes true, inhibiting the clock from setting the flip-flop true. At the end of the preset pulse, the clock resets the flip-

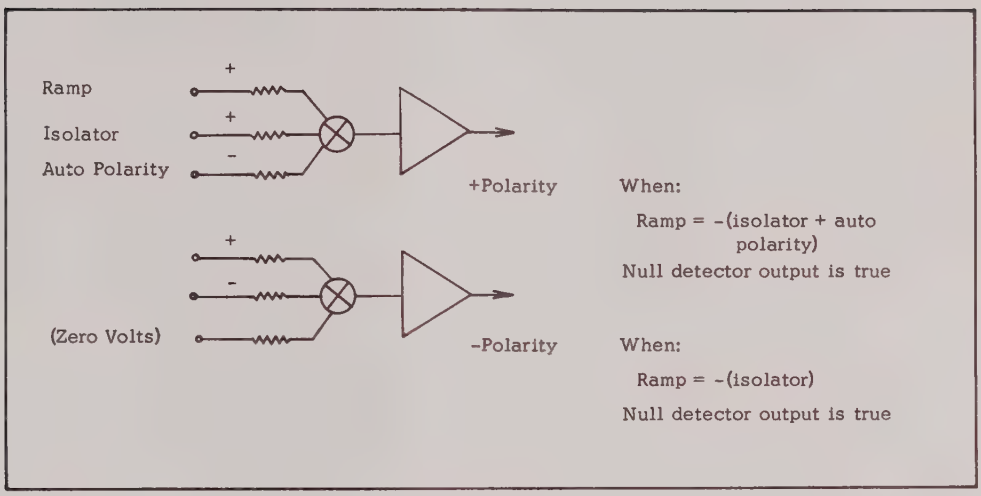


Figure 4.8. Null Detector

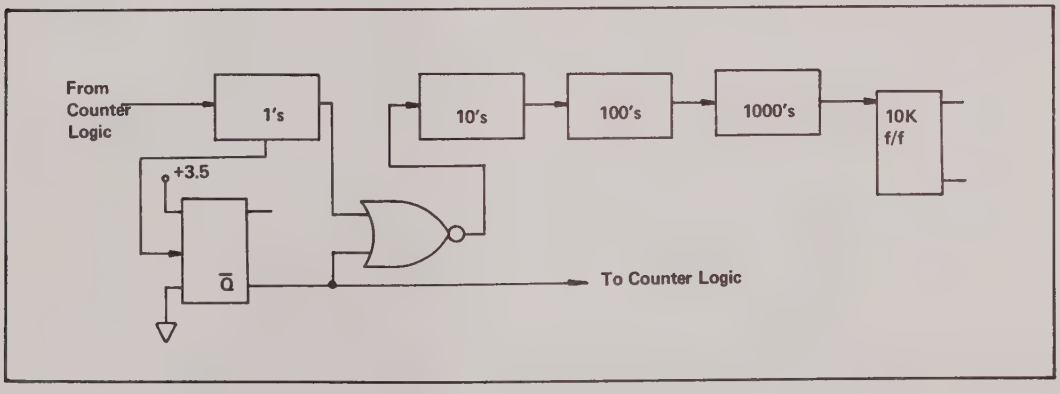


Figure 4.9. Binary Counter

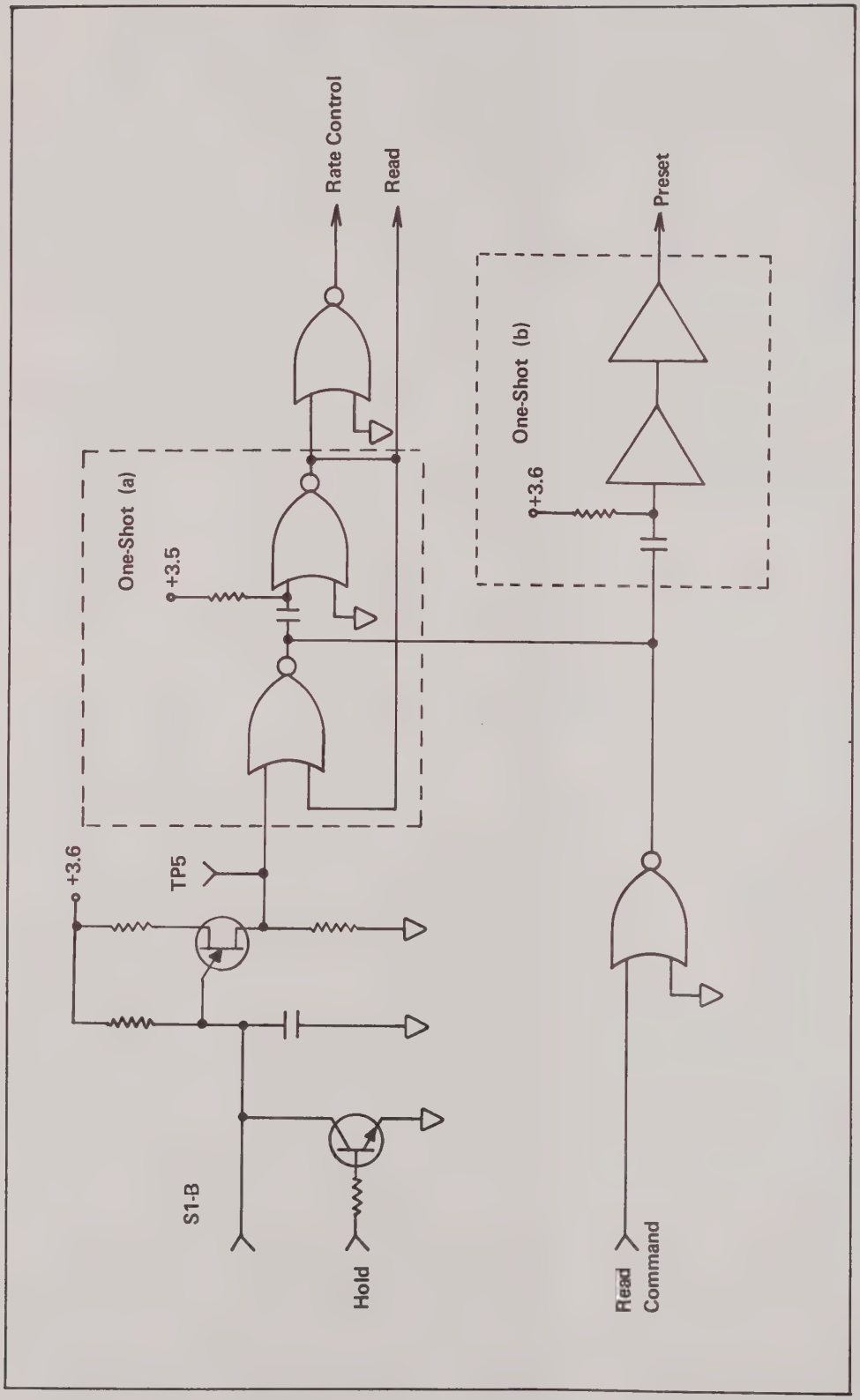


Figure 4.10. Rate Control

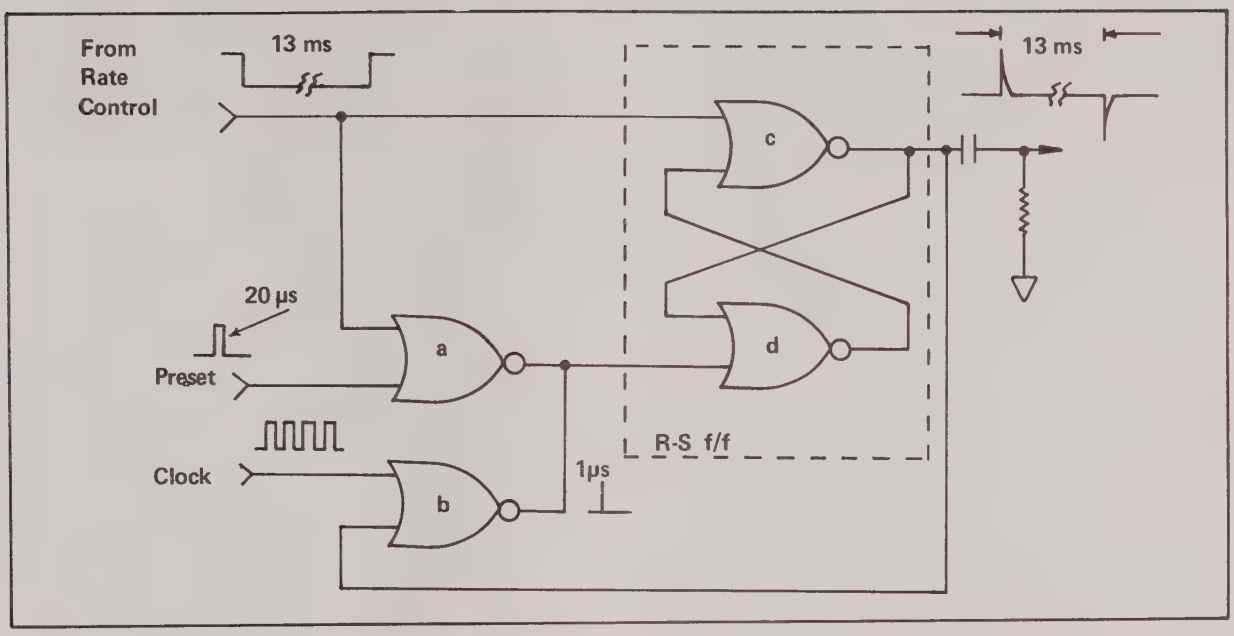


Figure 4.11. Read Control Circuitry

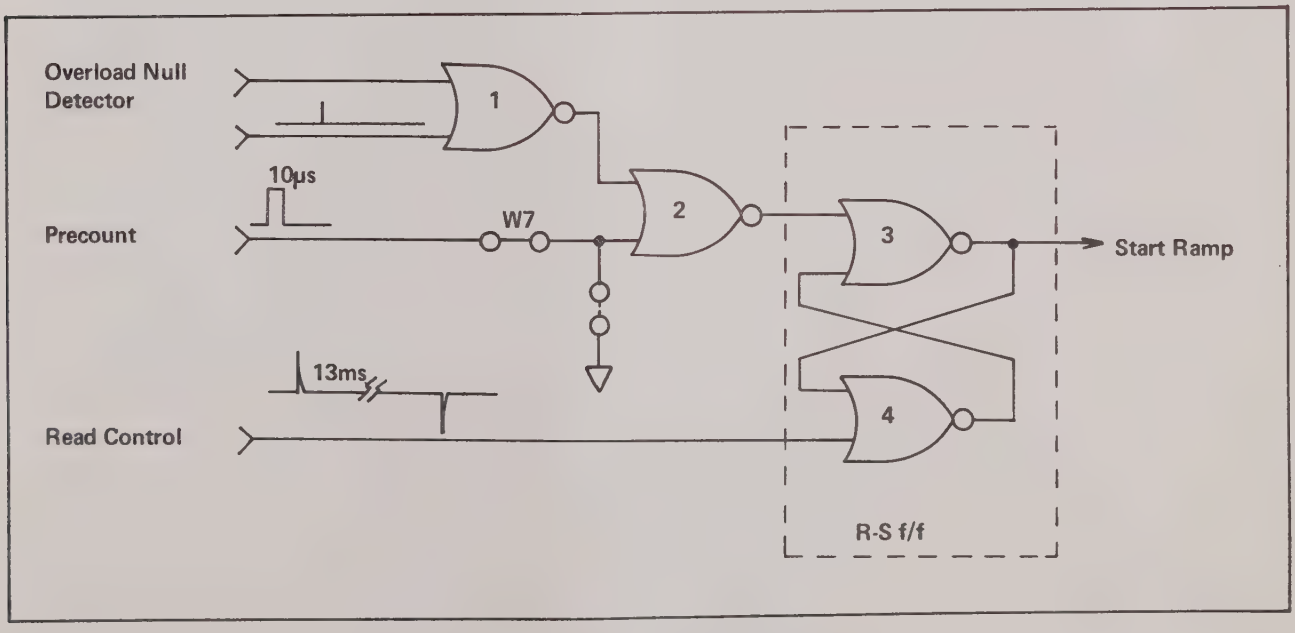


Figure 4.12. Ramp Control

flop. As the flip-flop goes true, the clock pulse is again inhibited, this time by the positive bias at NOR gate (b). The flip-flop remains true for the remainder of the rate control output. The read control flip-flop output is differentiated by an RC network before being applied to the ramp control circuit.

4.39. Ramp Control. The ramp control (figure 4.12) starts and stops the ramp generator. It also controls the blanking circuit and enables the counter control.

4.40. The ramp control flip-flop is set true by the positive-going edge of the read control output. During the precount of the digital counter, the ramp control flip-flop is inhibited from being reset by a precount signal ($\overline{Q}$ of the precount f/f) at the input of NOR gate (2). The flip-flop is then reset on the receipt of a Null Detector output signal or an overload signal at the input of NOR gate (1).

4.41. Counter Control. The counter control circuit (figure 4.13) inhibits the clock train from driving the binary counter until the start ramp goes true.

4.42 BLANKING CIRCUIT

4.43. The blanking circuit lowers the positive supply voltage to the readout tubes causing them to extinguish or blank. Blanking occurs when the start ramp is positive, causing the blanking transistor to conduct.

4.44 RANGE LOGIC (Figure 4.14)

4.45. The range logic generates the information required by the auto range circuitry of the Accessory Module to produce a range change. An up range signal is generated by a logic false appearing at both inputs of NOR gate (a): $\overline{\text{OVERLOAD}}$ and HIGHEST RANGE. $\overline{\text{OVERLOAD}}$ is the $\overline{Q}$ output of the overload flip-flop and is false in an overload condition. HIGHEST RANGE is false when an UP range is possible.

4.46. A down range signal is generated by a logic false appearing at both inputs of NOR gate (b): LOWEST RANGE and the Q output of the DOWN range flip-flop. LOWEST RANGE is false if a DOWN range is possible and Q is set false at the start of a read cycle by the reset pulse. The DOWN

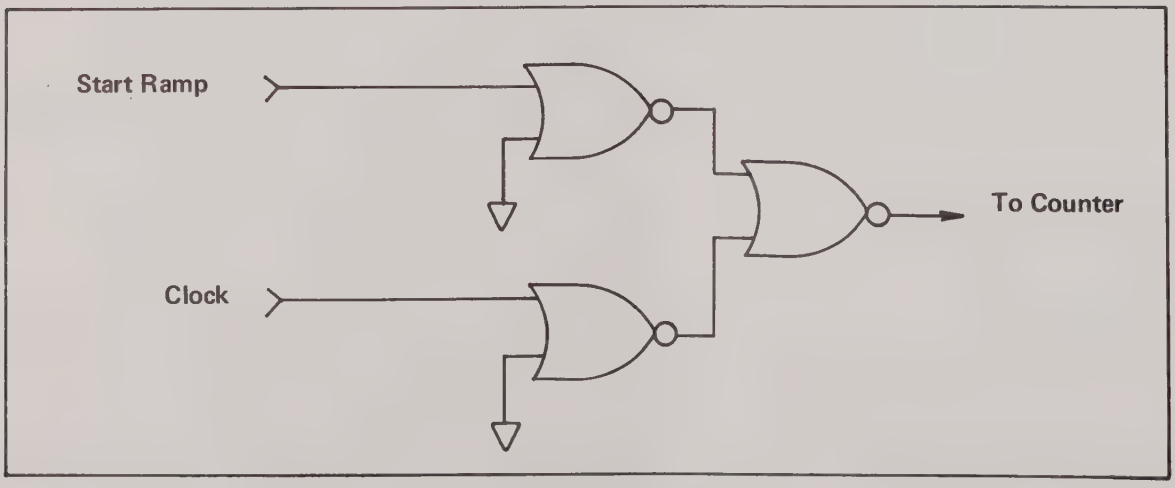


Figure 4.13. Counter Control

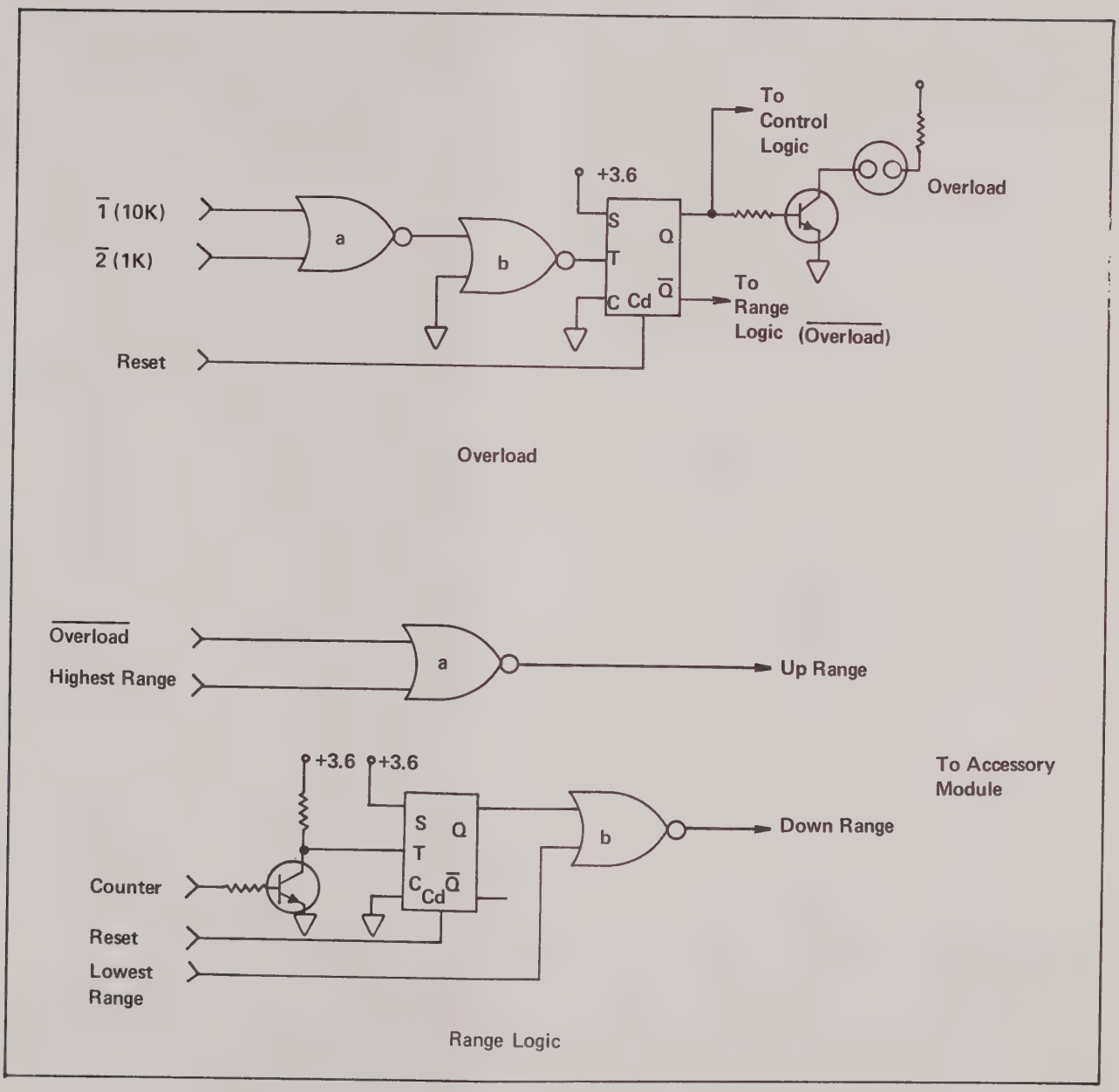


Figure 4.14. Overload and Range Logic

range signal is true until the counter reaches 1000. The flip-flop is set by an inverted signal from the counter. The inverted signal goes true at a count of eight hundred and false again at a count of one thousand, the negative side of the pulse setting Q to logic true.

4.47. Notice that the UP range remains false even in an overload condition when the instrument is in the highest range and the DOWN range remains false during a read cycle when the instrument is in the lowest range.

4.48 OVERLOAD

4.49. The overload circuit detects when the digital counter has reached 12,000 or full scale. A signal is sent to the control logic and the overload indicator lights.

4.50. At the beginning of a reading, the reset pulse sets Q false and $\overline{Q}$ true. The inputs of NOR gate (a) consist of $\overline{2}$ (not 2) of the 1K decade and $\overline{1}$ (not 1) of the 10K flip-flop (actually the zero driver side of the flip-flop). Either one or both of these inputs are true until the counter reaches 12,000. At this time, the output of NOR gate (a) negative-going edge of this pulse causes the overload flip-flop to change state (Q goes true and $\overline{Q}$ goes false). The positive level at Q drives the overload indicator on and signals the control logic to stop the counter and ramp. $\overline{Q}$ is used by the range logic.

4.51 POLARITY SENSE (Figure 4.15)

4.52. The polarity sense circuitry controls the polarity indicator. The Auto Polarity, which automatically compensates for changes in polarity of the input signal, drives the single-staged differential amplifier of the polarity sense circuit. The outputs of the amplifier drive the set (s) and the clear (c) inputs of the J/K flip-flop. The negative going side of the read pulse (following the read cycle) signals the flip-flop to change state if required.

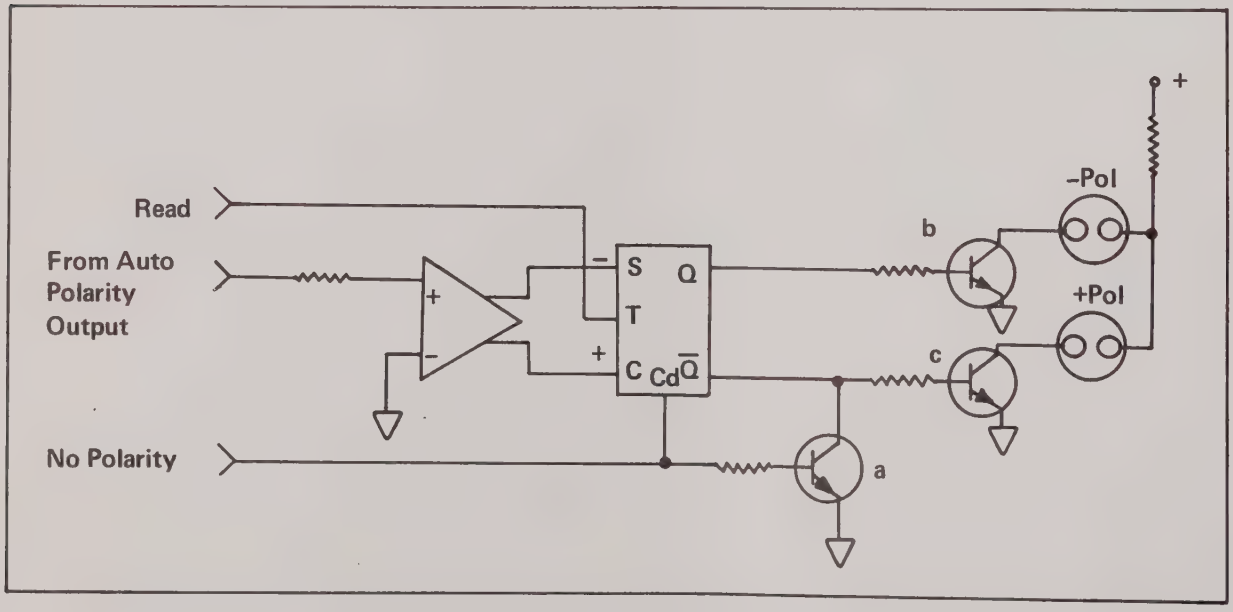


Figure 4.15. Polarity Sense

The flip-flop outputs Q and $\overline{Q}$ control the driver transistors of the minus and plus polarity indicators. The NO POLARITY input is set true when AC is selected. The positive bias at Cd forces Q false and transistor (a) shunts $\overline{Q}$ to false, causing both the minus and plus polarity indicators to remain off.

4.53 CLOCK

4.54. The clock circuit produces a symmetrical 1 MHz stable timing signal for driving the counter circuit.

4.55. The circuit, as shown in figure 4.16, uses two NOR gates interconnected to form a crystal controlled free-running multivibrator. Referring to figure 4.31 the oscillator operates as follows: Assume e1 is false, biasing Q4 off. C is driven negative, turning Q3 off and causing e2 to go true. e2 at true biases Q1 on. C charges positively through R2 until Q3 is biased on (approximately 0.85 volts). At this time, e2 goes false, Q1 is biased off and Q2 is driven off by crystal (x) being driven negative. With both transistors Q1 and Q2 driven off, e1 goes true, biasing Q4 on. R1 charges X until Q2 turns on, setting e1 to false. The operation then repeats itself.

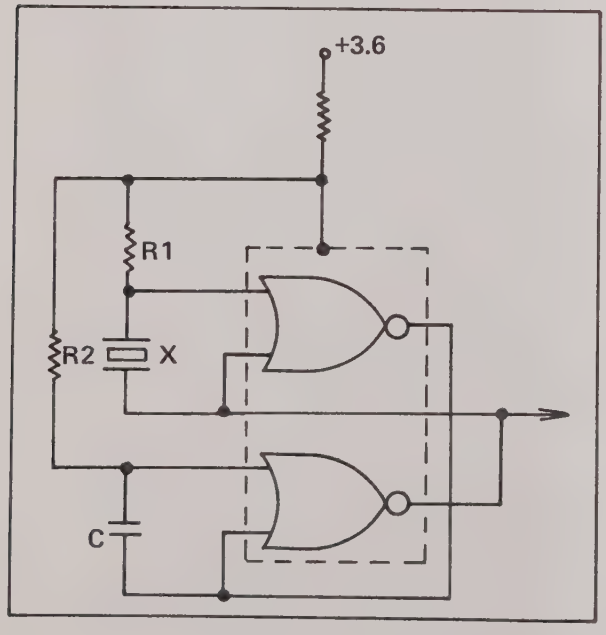


Figure 4.16. Clock

4.56 BCD TO DECIMAL DECODING

4.57. The four J-K flip-flops, A_1, A_2, B_1, and B_2 (figure 4.17) drive the BCD-to-decimal converter and carry the logic weights of 1, 2, 4, and 8, respectively. The four flip-flops and two NOR gates are interconnected to convert ten input pulses into ten separate BCD coded outputs ranging in numerical value from zero to nine.

4.58. At the beginning of a read cycle, the reset pulse is applied to all of the counter flip-flops, setting the outputs false (negative true logic). The logic levels of various points in the counter are shown in the timing diagram of figure 4.17.

4.59 POWER SUPPLY

4.60. 3.6 Volt Supply. The +3.6 volt supply is used by all of the micrologic circuitry and in circuits used to directly drive the integrated circuits.

4.61. As shown in figure 4.18, voltage to the supply is provided by a full wave rectified 8 volts from a center-tapped secondary and diodes CR5 and CR6. Reference for the supply is taken from across zener diode CR11. The zener voltage is compared with a fractional part of the output voltage and the error signal used to drive a Darlington coupled emitter follower, Q2 and Q3. The output voltage is taken from the emitter of Q3 and added regulation is provided by capacitor C16.

4.62. High Voltage Supplies. The 300-volt supply provides the anode potential for the nixie readout

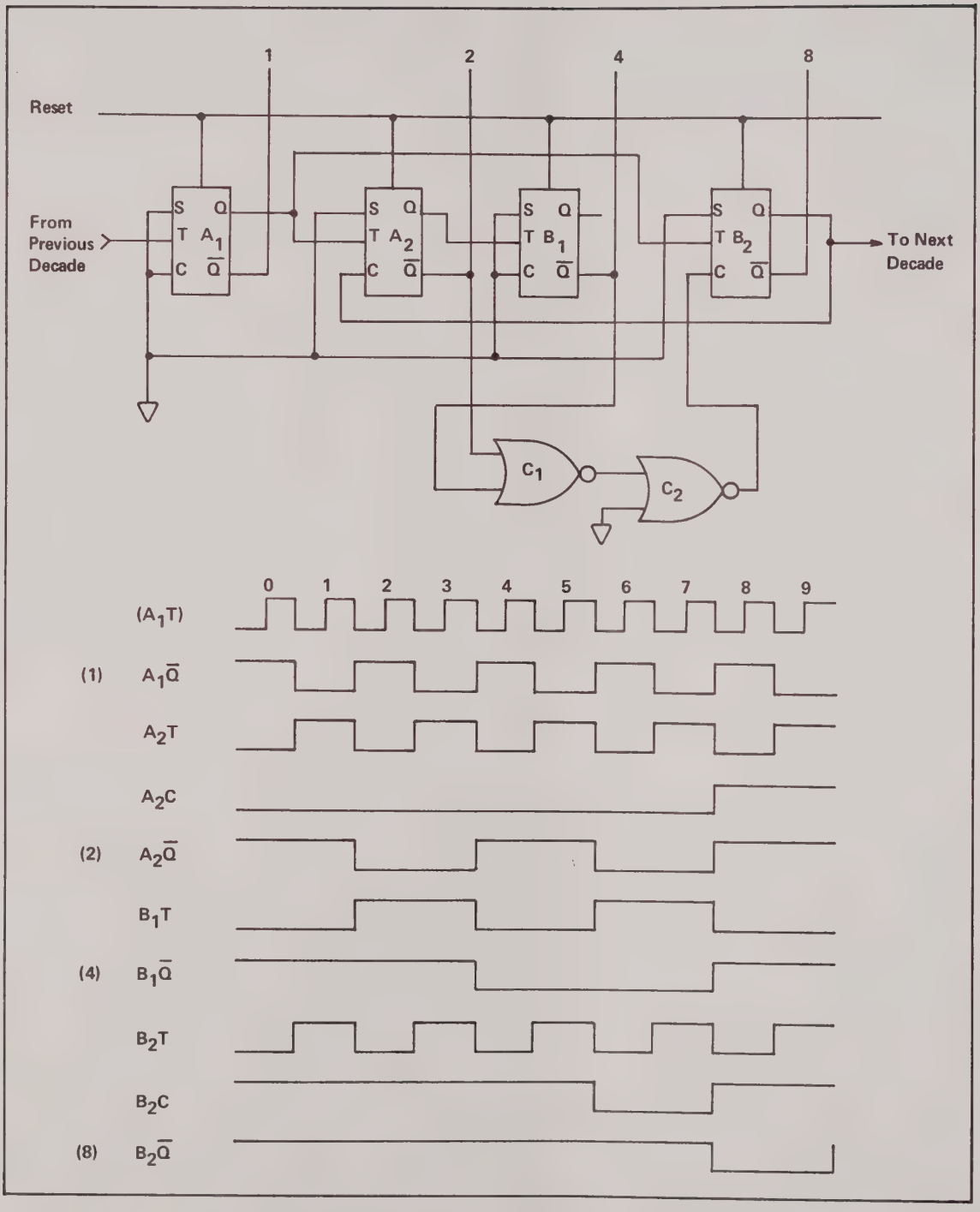


Figure 4-17. BCD - Decimal Conversion

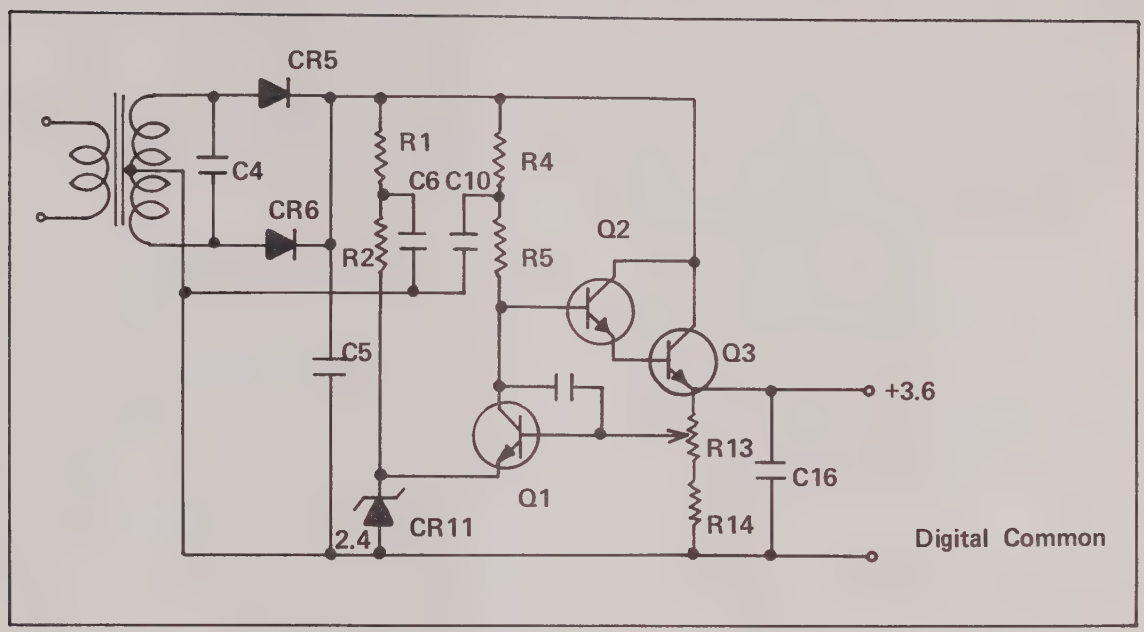


Figure 4.18. 3.6-Volt Supply

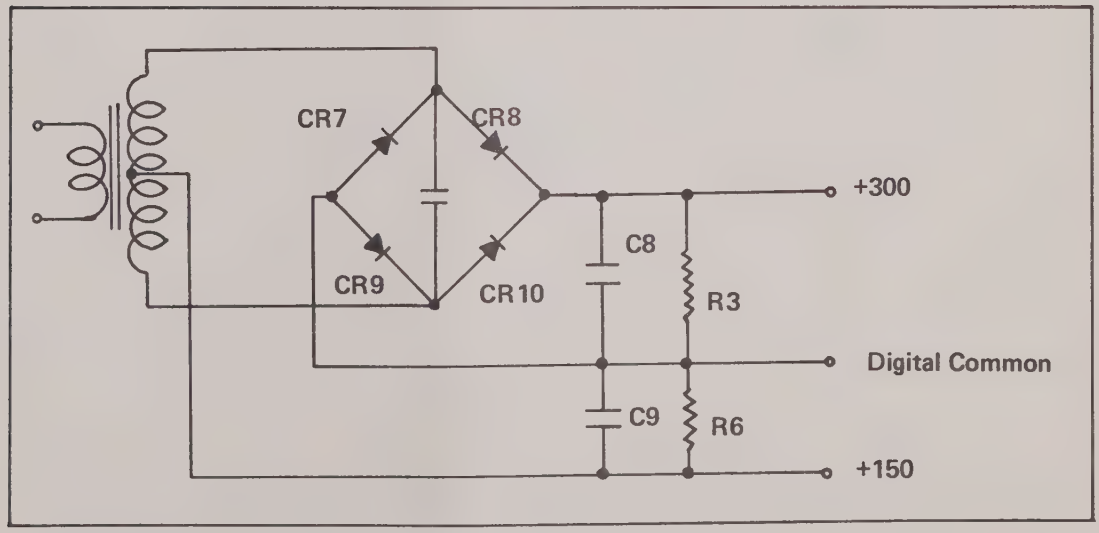


Figure 4.19. High Voltage Supply

tubes. The 150-volt supply provides the required potential for operating the polarity and overload indicators.

4.63. As shown in figure 4.19, the 300-volt output is generated across the bridge rectifier consisting of diodes CR7, CR8, CR9, and CR10. Capacitor C8 provides filtering. The 150-volt output is taken from the center tap of the secondary used for the 300-volt supply. Diodes CR7 and CR9 carry the current of both the 300 and 150-volt supplies. Filtering for the 150-volt output is provided by C9. Commons for all three supplies are tied together.

4.64. 28 Volt Supplies. The plus and minus 28 volt supplies are used both in the Accessory Module and in the analog circuits of the Digitizing and Display module.

4.65. Referring to figure 4.20, diodes CR2 and CR4, in conjunction with the secondard winding center tap, form the full-wave rectified +28 volt supply. The -28 volt supply uses the same center tap and diodes CR1 and CR3. Capacitor C2 and C3 are used for filtering.

4.66. 18 Volt Supplies. The plus and minus 18 volt supplies are regulated and are used in the same areas of the DMM as the 28 volt supplies.

4.67. Rectified voltage to power the 18 volt supplies is provided by the plus and minus 28 volt supplies. In the +18 volt supply, zener diode CR12 provides a reference of approximately 18.5 volts which is applied to the base of emitter follower Q4. The +18 volts is taken directly from the emitter of Q4 and current from the supply is limited by collector resistor R8. The -18 volt supply uses the same principle as the +18 volt supply. Reference is taken from zener diode CR13 and the -18 volts is taken from the emitter of Q5.

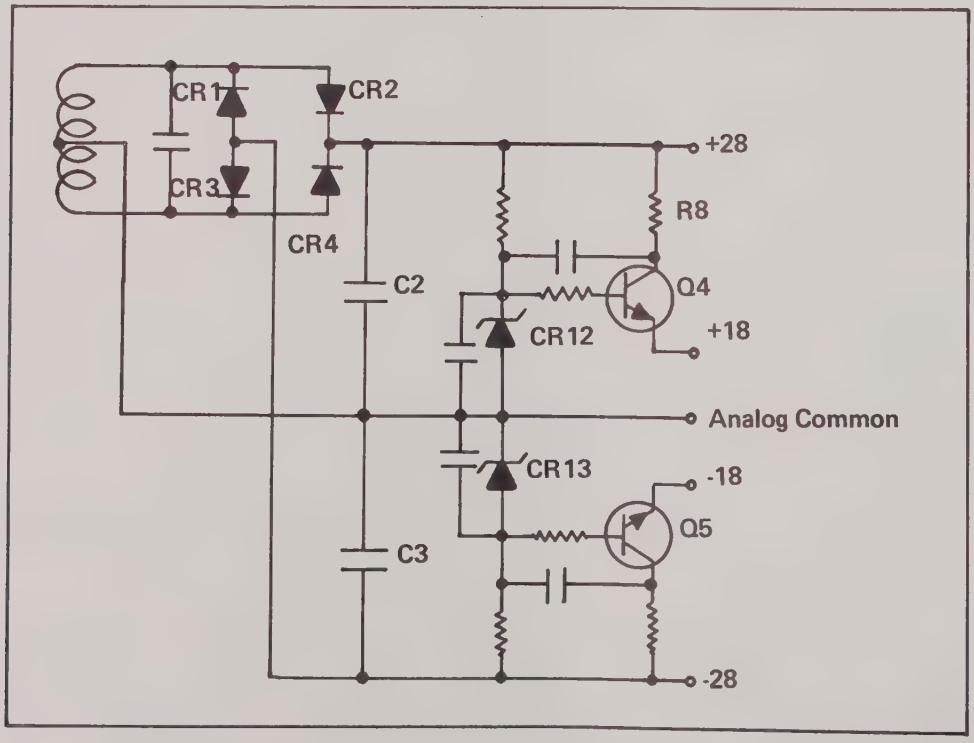


Figure 4.20. 28-Volt Supply

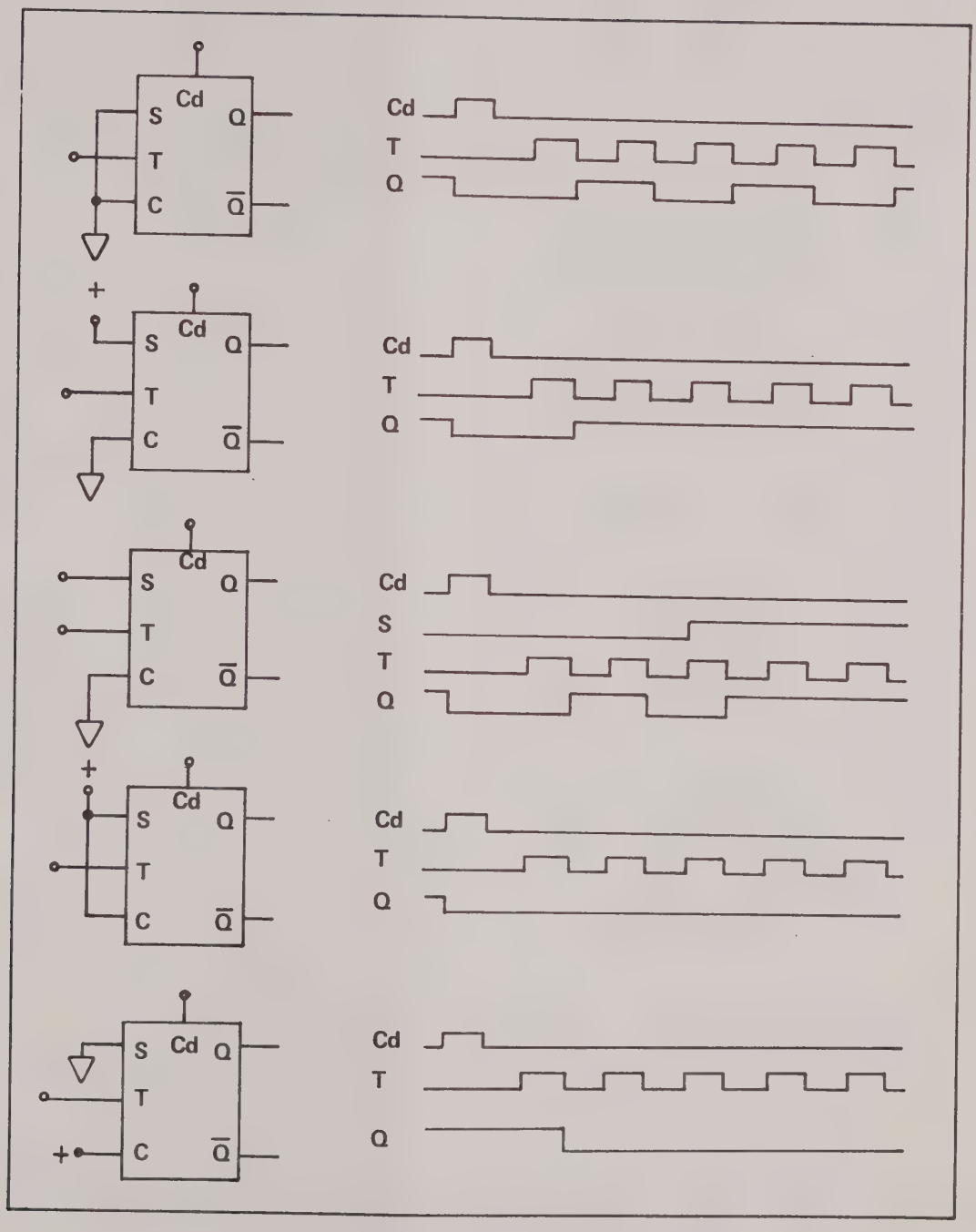


Figure 4.21. Flip-Flop Operating Modes

4.68 INTEGRATED CIRCUIT ELEMENTS

4.69. The following basic integrated circuits are used in the DMM:

MC723P	J-K Flip-flop
MC790P	Dual J-K Flip-flop
CML9960	Decoder Display Driver
MC799P	Dual Buffer
MC724P	Quad Two-input NOR Gate
MC717P	Quad Two-input NOR Gate

4.70. The physical and mechanical characteristics of each of the basic elements are tabulated in figures 4.26 through 4.30 at the end of this section.

4.71 J-K FLIP-FLOP OPERATING MODES

4.72. Shown in figure 4.21 are five common modes of operating the J-K flip-flop in the Series 4400 DMM. Output Q, prior to receipt of the Cd pulse, is determined by the previous state of the flip-flop. Output $\overline{Q}$ is the inverse of Q.

4.73. Figure 4.22 shows the interconnecting of the two NOR gates so as to obtain an R-S flip-flop.

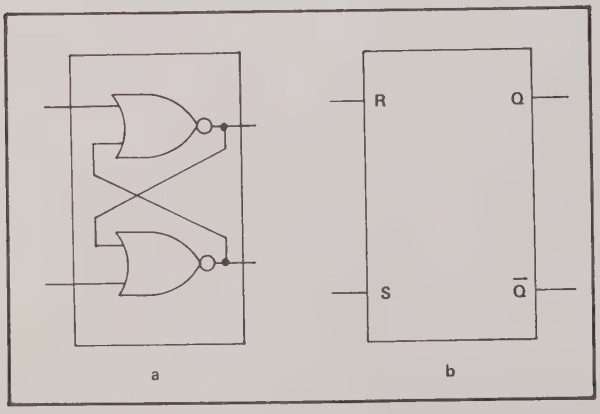


Figure 4.22. Interconnected Nor Gates

4.74 SCHEMATIC IDENTIFICATION OF LOGIC DEVICES

4.75. Reference designators for all devices regardless of type have the letter "M" as a designating letter. This is followed by a number to identify the component uniquely (figure 4.23).

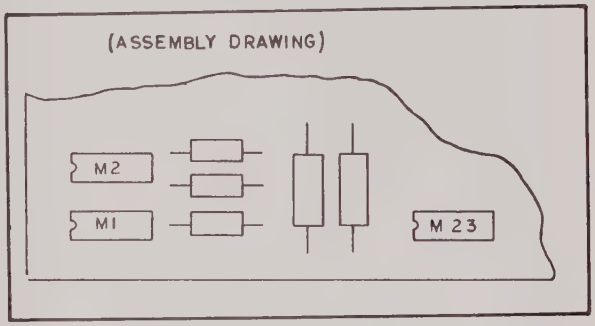


Figure 4.23. Component Identification

4.76. Identification of Logic Function Symbols. Individual logic functions are identified on the schematic by the designator of the logic device in which they appear. In most cases, circuitry for more than one function is encased within the same module. To distinguish between them, an additional letter designator is affixed to that of the device (A, B, C, D, etc.), as required to cover all functions (figure 4.24).

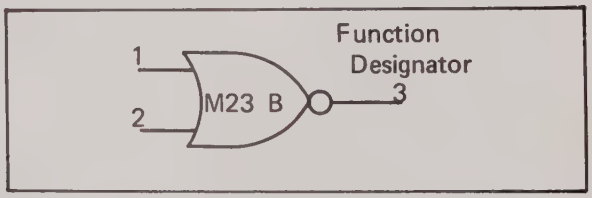


Figure 4.24. Function Designator

4.77. Input-Output Pin Numbers. Module pin numbers are placed outside the function symbols next to the input and output leads.

4.78. Identifying Type of Device. Module (IC element) type is defined on the schematic in note

form. This applies, of course, to the major type used on the schematic. If more than one type of device is used for the same logic function, the least used is defined at the logic symbol.

4.79. Circuit Definition of Logic Devices. A circuit diagram of the logic devices used does not appear on each schematic; rather, schematics in figures 4.26 through 4.30 describe all elements used.

4.80. Restriction on Logic Symbol Usage. On schematics that contain both integrated circuit elements and discrete components, the logic symbols describe only that circuitry which is contained within the devices. In other words, no logic symbols are used to represent a function that is made up of discrete components.

4.81. Standard Symbols. Figure 4.25 shows the standard integrated circuit logic symbols used on Dana drawings.

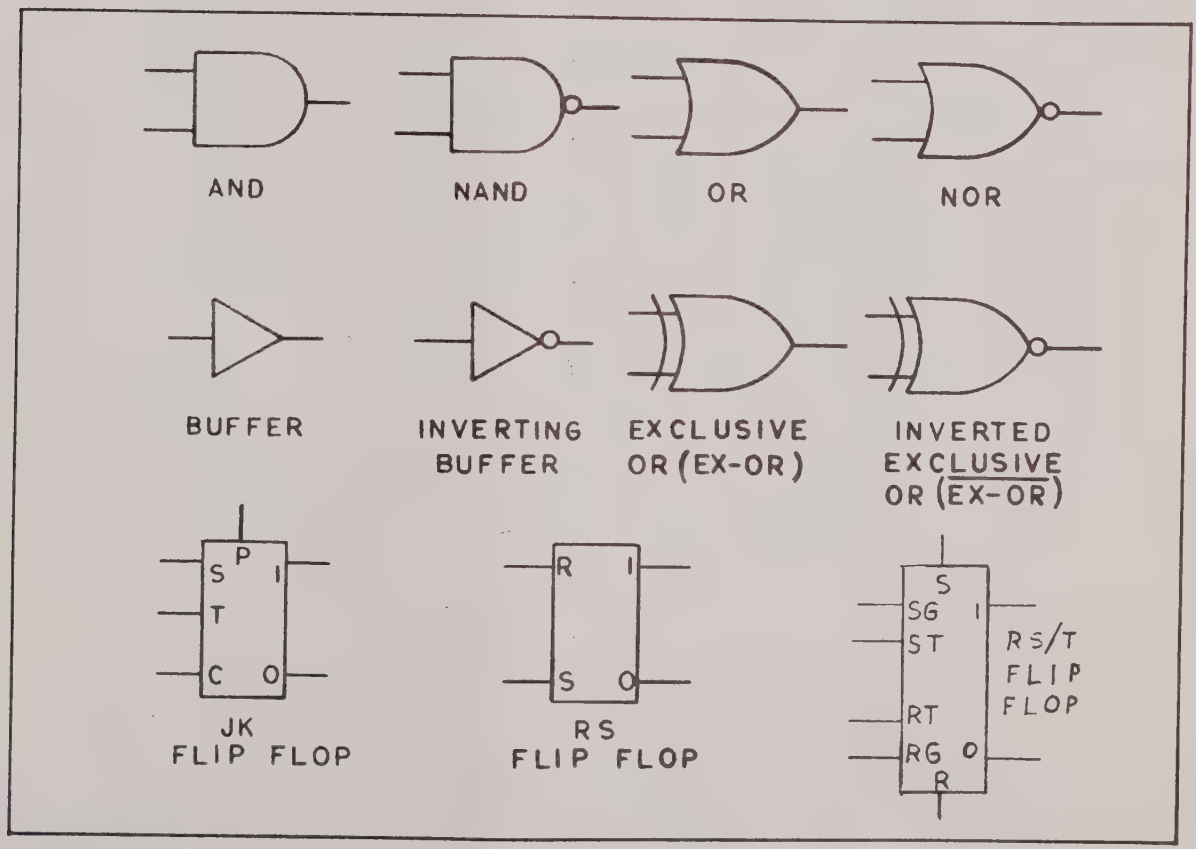
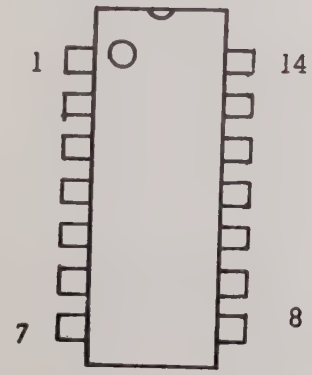


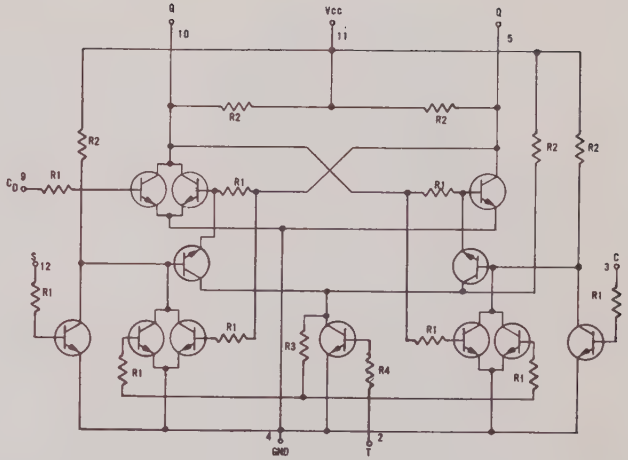
Figure 4.25. Logic Symbols

MC 723P J-K Flip-Flop	
R_1	450 Ohms
R_2	640 Ohms
R_3	510 Ohms
R_4	225 Ohms
f_{tog}	4 mHz
V_{off}	+0.46V Max
V_{on}	+0.85V Min
V_{out}	+0.3V Max
Vcc	+3.6V ±10%



TN (NOTE 2)		TN+1 (NOTE 2)	
S	C	Q	$\overline{Q}$
1	1	QN^3	$\overline{Q}N$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}N$	QN^3

(Note 3)



NOTES:

1. Direct input Cd must be low.
2. The time period prior to the negative transition of the clock pulse is denoted Tn and the time period subsequent to this transition is denoted Tn+1.
3. Qn is the state of the Q output in the time period Tn.
4. Clock Pulse (T) inputs must have a fall time within the range of 10ns to 100ns. Fall time is a straightline function from 1V to ground.

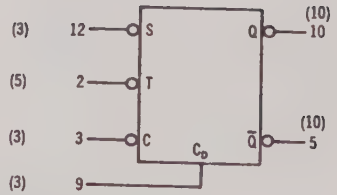
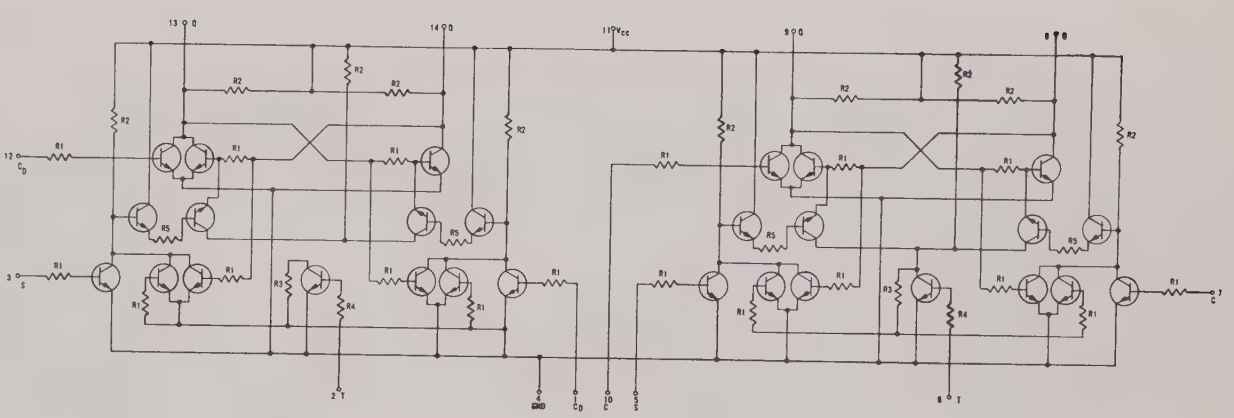


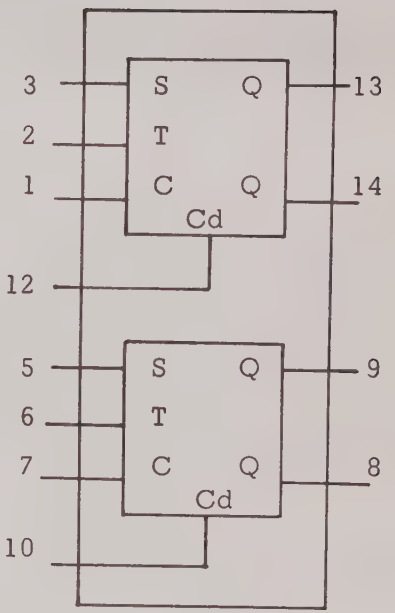
Figure 4.26. J-K Flip-Flop

MC 790 P Dual J-K Flip-Flop	
R_1	450 Ohms
R_2	640 Ohms
R_3	510 Ohms
R_4	225 Ohms
R_5	300 Ohms
V_{off}	+0.46V Max
V_{on}	+0.85V Min
V_{out}	+0.3V Max
Vcc	+3.6V ±10%
f_{tog}	4 mHz



TN (NOTE 2)		TN+1 (NOTE 2)	
S	C	Q	$\overline{Q}$
1	1	Q_N [3]	$\overline{Q}_N$
1	0	1	0
0	1	0	1
0	0	$\overline{Q}_N$	Q_N [3]

(Note 3)



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2. The time period prior to the negative transition of the clock pulse is denoted Tn and the time period subsequent to this transition is denoted Tn+1.
3. Qn is the state of the Q output in the time period Tn.
4. Clock Pulse (T) inputs must have a fall time within the range of 10ns to 100ns. Fall time is a straightline function from 1V to ground.

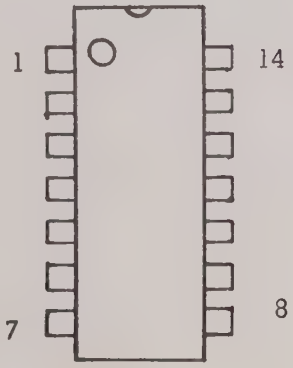
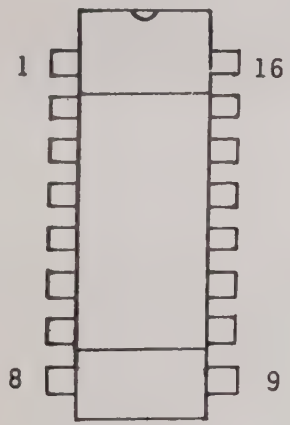
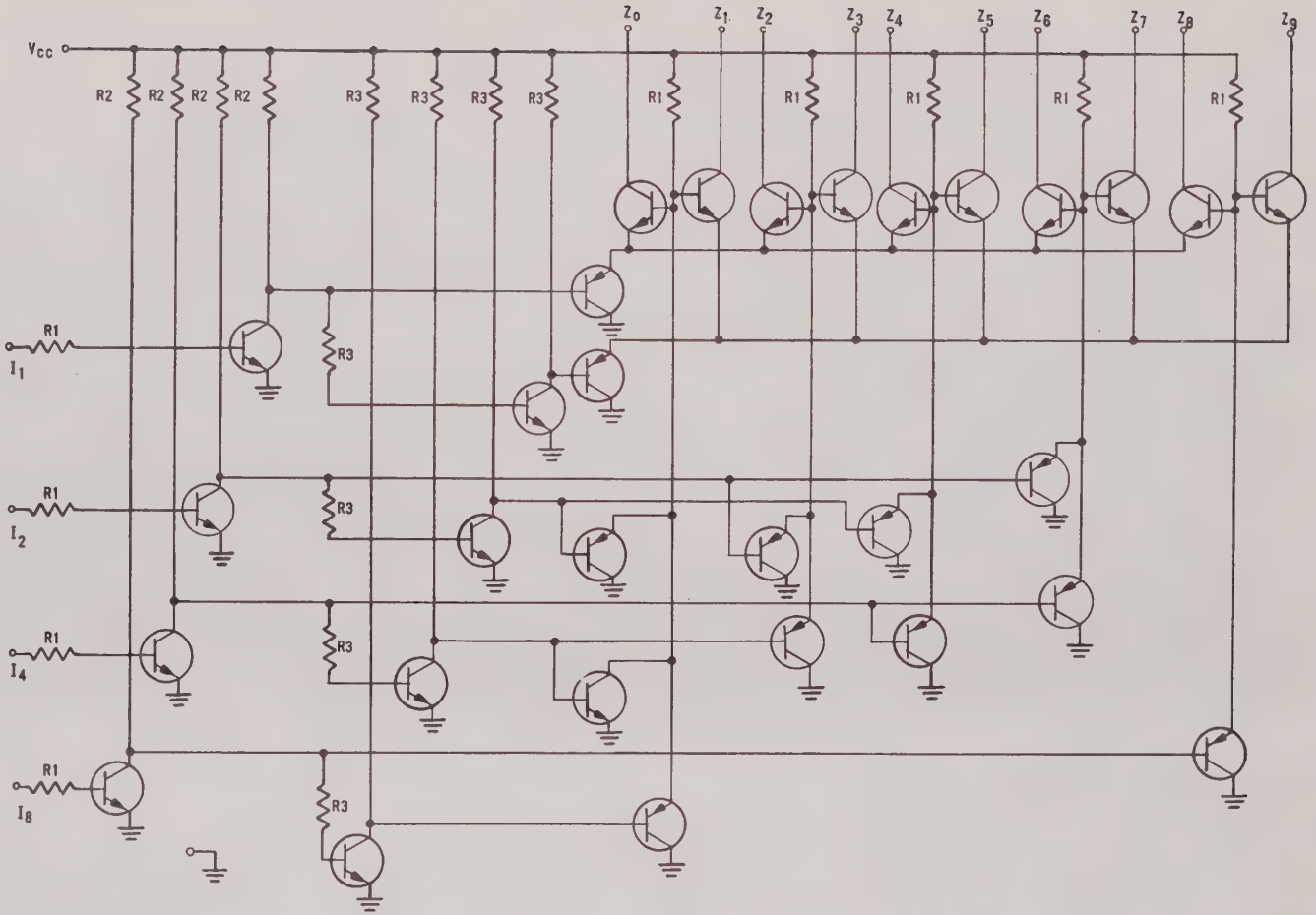
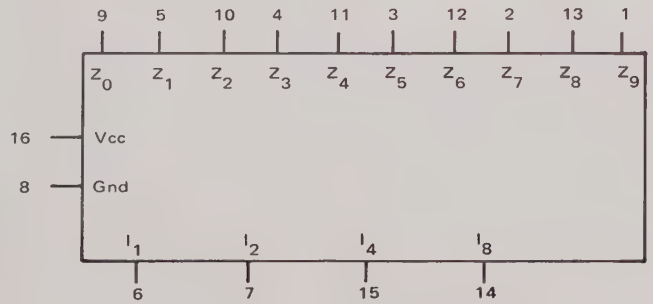


Figure 4.27. Dual J-K Flip-Flop

CML 9960 Decoder Display Driver	
R_1	2K
R_2	4K
R_3	5K
V_{off}	+0.4V Max
V_{on}	+1.0V Min
I_{out}	10.0 Ma Max
Vcc	+4.4V ±25%







Digit

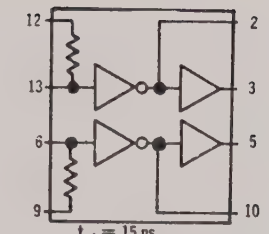
Input	0	1	2	3	4	5	6	7	8	9
1	1	0	1	0	1	0	1	0	1	0
2	1	1	0	0	1	1	0	0	1	1
4	1	1	1	1	0	0	0	0	1	1
8	1	1	1	1	1	1	1	1	0	0

1 = Vcc

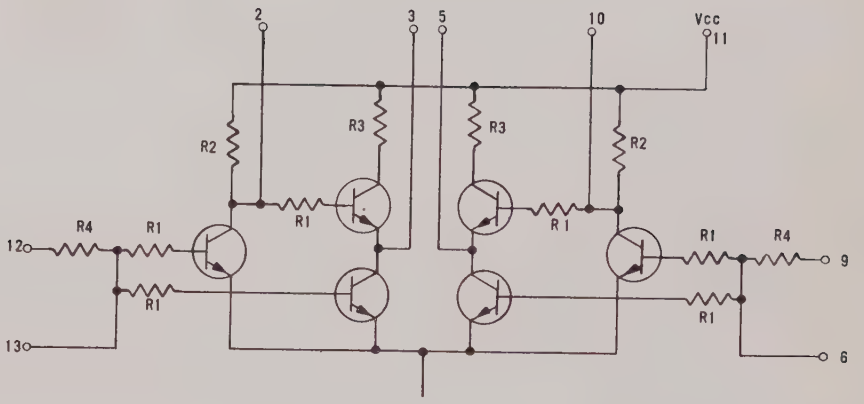
0 = Gnd

Figure 4.28. Decoder Display

MC 799P Dual Buffer	
R_1	450 Ohms
R_2	640 Ohms
R_3	100 Ohms
R_4	1000 Ohms
V_{off}	+0.46V Max
V_{on}	+0.85V Min
V_{out}	+0.3V Max
Vcc	+3.6V ±10%



Outputs 2 and 3 may not be used simultaneously.
Outputs 5 and 10 may not be used simultaneously.



Input					Output			
12	13	6	9		2	3	5	10
0					1			
1					0			
	0					1		
	1					0		
		0					1	
		1					0	
			0					1
			1					0

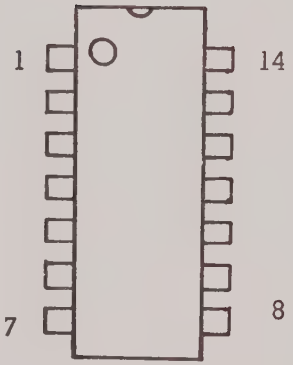
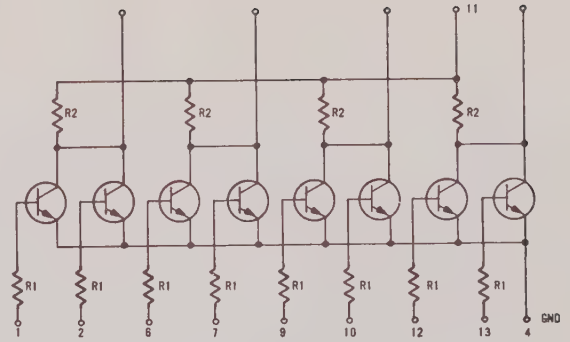


Figure 4.29. Dual Buffer

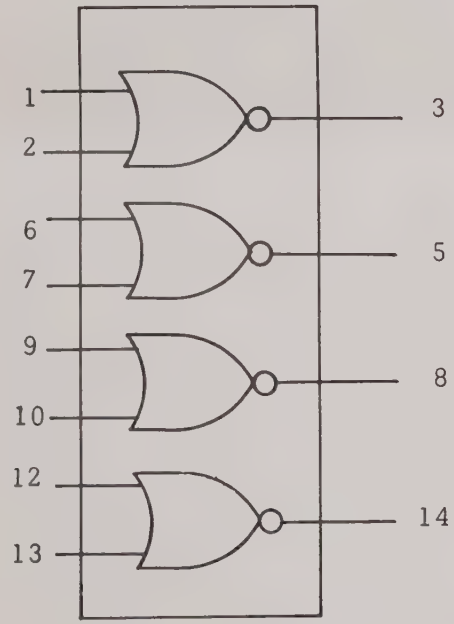
MC 717P
MC 724

QUAD 2-INPUT NOR GATE

	MC717P	MC724P
R_1	1.5K	450 Ohms
R_2	3.6K	640 Ohms
V_{off}	0.46 Max	
V_{on}	0.85 Min	
V_{out}	0.3 Max	
Vcc	3.6 ±10%	



Inputs								Output			
1	2	6	7	9	10	12	13	3	5	8	14
0	0							1			
1	0							0			
0	1							0			
1	1							0			
		0	0						1		
		1	0						0		
		0	1						0		
		1	1						0		
				0	0					1	
				1	0					0	
				0	1					0	
				1	1					0	
						0	0				1
						1	0				0
						0	1				0
						1	1				0



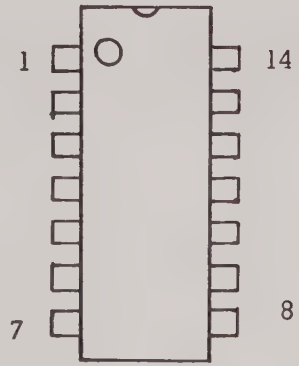


Figure 4.30. Quad Two-Input Nor Gate

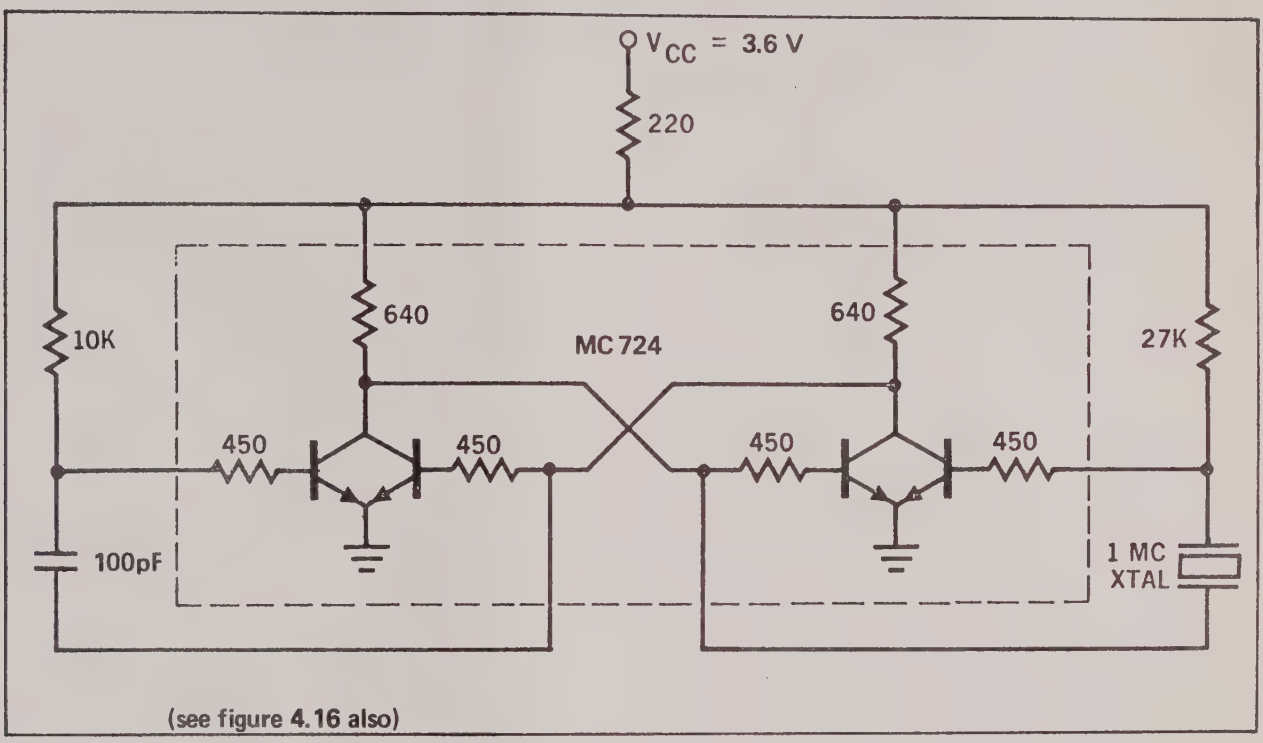


Figure 4.31. MC724 Used as a Crystal Oscillator

SECTION 5

CALIBRATION

5.1 INTRODUCTION

5.2 General. This calibration procedure is designed for normal periodic adjustment to return the instrument to its original factory performance. Any necessary maintenance should be done prior to calibration. Each calibration step in this procedure relies on the accuracy of the preceding step. Care should be taken to make each adjustment in the order that appears in this procedure.

5.3 EQUIPMENT

5.4. General. The following equipment is required for DMM calibration, and is listed in order of use. The specifications listed are the minimum required to make the adjustment, not the accuracy of the instrument mentioned. Equipment required for the calibration of the Digitizing and Display portion and the DC portion of the accessory module are listed below.

(a) Precision null detector/microvoltmeter with a minimum of 10 microvolts of resolution. For example, Fluke Model 845AR.

(b) Voltage calibrator variable from 0 to 1000 volts and a resolution better than 100 microvolts (at 1 and 10 volts). For example, Fluke Model 332A.

(Paragraph 5.5 deleted)

5.6 TOOLS

(a) Insulated blade-type calibration tool.

(b) No. 1 Phillips screwdriver.

5.7 OTHER

(a) 10,000 ohm ¼ watt, 5% carbon resistor.

(b) 51,000 ohm ¼ watt, 5% carbon resistor.

5.8. This section combines the calibration adjustments for the Digitizing and Display portion with the Accessory portion. If desired, one portion, the Accessory Module for example, can be calibrated separately, provided that the other portion is known to be calibrated. Each calibration adjust heading is clearly marked whether for Digitizing and Display, Accessory, or Accessory Module 212.

5.9 PREPARATION

(a) Accessory Module. Remove the Accessory Module from the DMM and remove the module's top shield plate. Remount the module in the DMM, and select the 10 volt range.

(b) Remove both the top and bottom covers of the DMM. Set the Model 4400 OFF-

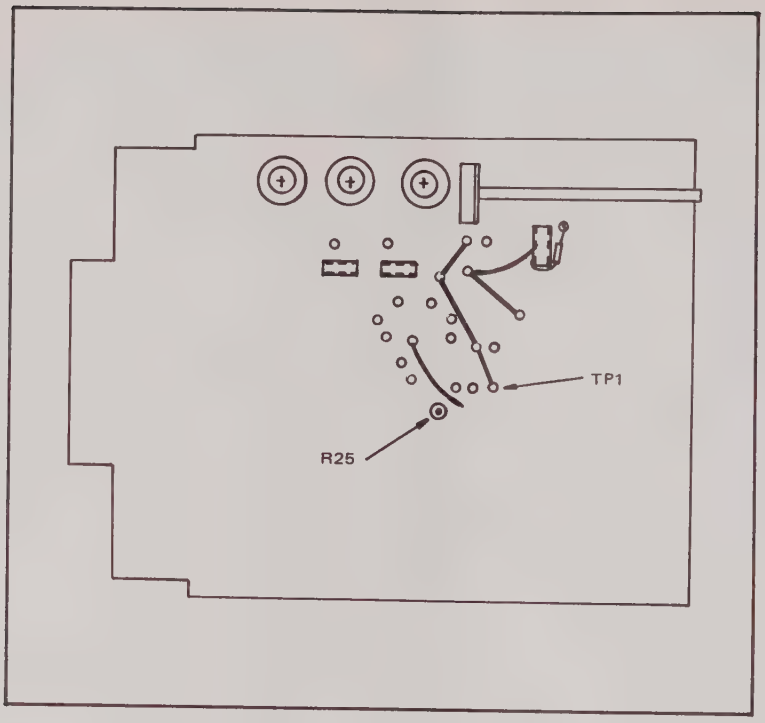


Figure 5.1. Locations - 212 Module (Bottom View)

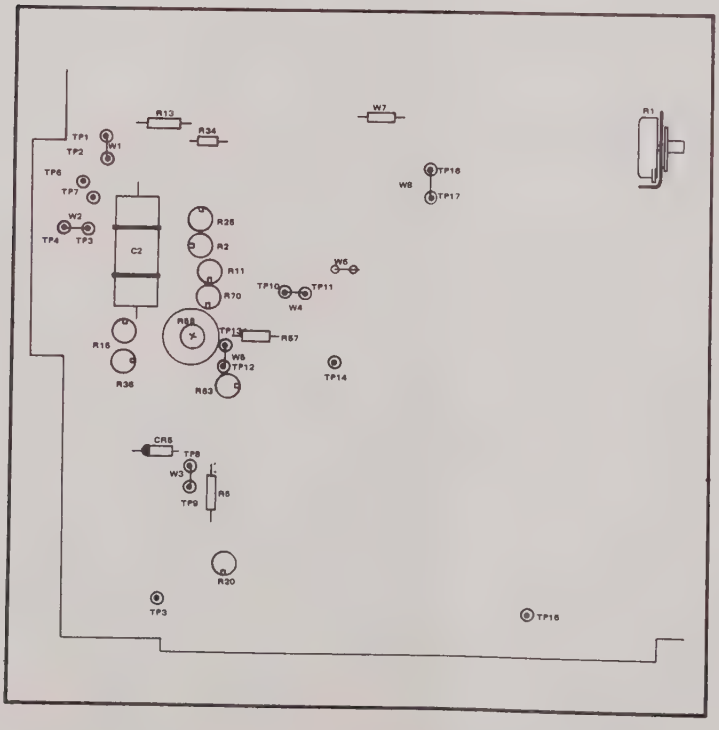


Figure 5.2. Locations, Digitizing & Display

ON-HOLD switch to ON and allow at least 30 minutes for the instrument to warm up.

5.10 SET UP INTERNAL REFERENCE VOLTAGE (Display Module)

(a) Set the precision voltage source output to value of the reference voltage as recorded on the zener serial tag (mounted on the back of the nixie shield).

(b) As shown in figure 5.3, connect the positive side of the voltage source to TP6 and the high side of the microvoltmeter to TP7 on the DMM display board. Connect the negative side of the voltage source to the low side of the microvoltmeter and tie the case connections together.

5.11 ADJUST INTERNAL REFERENCE (Display Module)

(a) An error voltage greater than 100 microvolts indicates the need to readjust the zener current supply.

(b) Adjust the zener current supply calibration potentiometer R36 for a microvoltmeter reading of zero ±10 microvolts.

(c) Remove the leads from TP6 and TP7.

5.12 ADJUST NULL DETECTOR ZERO (Display Module)

(a) Open connections W3, W4, and W5.

(b) Connect a jumper from TP6 to TP10.

(c) Connect the microvoltmeter common to TP6 and its input to the junction of resistors R57, R58 and R59.

(d) Adjust the current zero control R63 for zero ±10 microvolts.

(e) Remove jumpers and reconnect W3, W4, and W5.

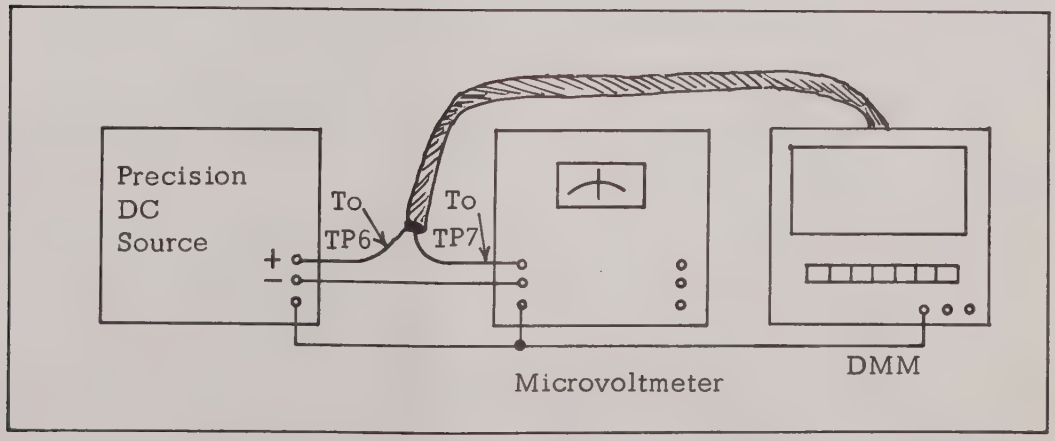


Figure 5.3. Test Setup - Reference Voltage

5.13 ADJUST RAMP GENERATOR ZERO (Display Module)

(a) Test setup is shown in figure 5.4.

(b) Open connection W2 (-6 volt reference).

(c) Connect a 10K ohm resistor across capacitor C2.

(d) Lift either end of FSV resistor R34.

(e) Connect a jumper from the left side of R13 (figure 5.2) to TP6. Connect the microvoltmeter common to TP6 and its input (in series with a 51K ohms resistor) to the top of capacitor C2 (see figure 5.2).

(f) Adjust the voltage zero control R25 for zero ±30 microvolts.

(g) Connect microvoltmeter input to the bottom of capacitor C2.

(h) Adjust the current zero control R11 for a microvoltmeter reading of zero ±30 microvolts.

(i) Remove jumper from R13 to TP6. Reconnect FSV resistor R34.

(j) Remove jumper and 10K ohm resistor. Remove the microvoltmeter leads and replace W2.

5.14 ADJUST DC ISOLATOR ZERO (Accessory Module)

(a) Select the 0.1 volt scale.

(b) On the accessory board, connect a jumper from the DMM input common (white) to the input base of Q7 (TP1 as shown in figure 5.1).

(c) Connect a microvoltmeter between TP2 and TP6 on the readout board.

(d) Adjust R25 (100K potentiometer) for a microvoltmeter reading of 0 ± 200 microvolts (accessory module).

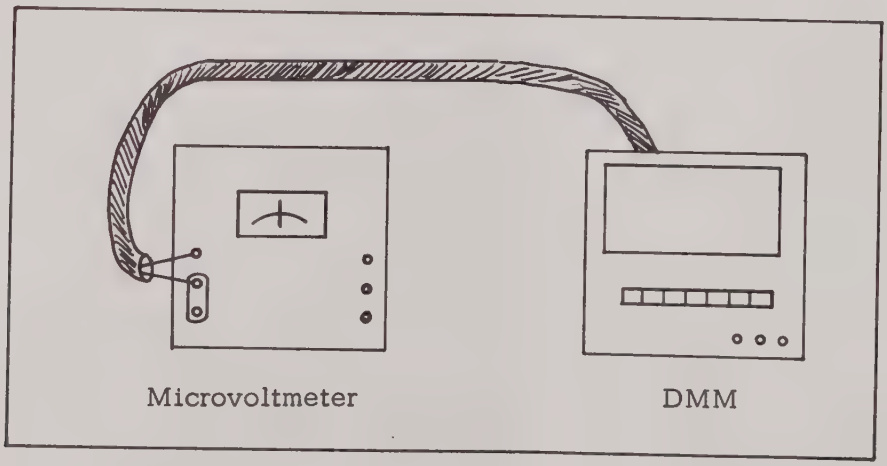


Figure 5.4. Test Setup - Ramp Zero

(e) Remove the jumper installed in step b. Connect a jumper across the two DMM input terminals (red and white).

(f) Adjust the front panel zero (R17) for a microvoltmeter reading of 0 ± 200 microvolts.

(g) Remove the microvoltmeter leads and remove the jumper across the DMM input terminals.

5.15 ADJUST DMM POLARITY (Display Module)

(a) Connect the DMM input terminals to a DC voltage source and set the voltage source output to -.002 volts.

(b) Adjust the null detector voltage zero control R70 for a display reading bouncing between -0.001 and -0.002 volts.

(c) Set input to +0.002 volts. Adjust R20 (voltage zero control for the auto polarity) for a display reading bouncing between 0.001 and 0.002 volts.

5.16 ADJUST POSITIVE AND NEGATIVE GAIN (Display Module)

(a) Set the calibrate control R1 on the front panel to its mechanical center.

(b) Set the voltage source output to -9.9990 volts.

(c) Adjust the rough calibration control R2 for a DMM display reading of 9.9 volts. Adjust R1 for a display reading bouncing between -9.998 and -9.999.

(d) Reverse the polarity of the voltage source (+9.9990).

(e) Adjust the positive polarity gain control R55 for a display reading bouncing between 9.998 and 9.999 volts.

(f) Repeat steps a through d for interaction between controls.

5.17 ADJUST VOLTAGE DIVIDER (Accessory Module)

(a) Set the voltage source output to -0.10000 volts and the DMM range to .1.

(b) Adjust the millivolt gain control R67 for a display of -.10000.

(c) Select the 1 volt range and set the voltage source to -1.00000.

(d) Adjust the 1 volt gain control R60 for a display of -1.0000.

(e) Select the 1000 volt range and set the voltage source to -1000.00.

(f) Adjust the 1000 volt divider control R4 for a display of -1000.0.

(g) Set the voltage source to 1 volt and remove the supply from the input terminals.

5.18 ADJUST CALIBRATE TEST (Display Module)

(a) Select a DMM range of 1.

(b) Manually depress and hold in the calibration switch.

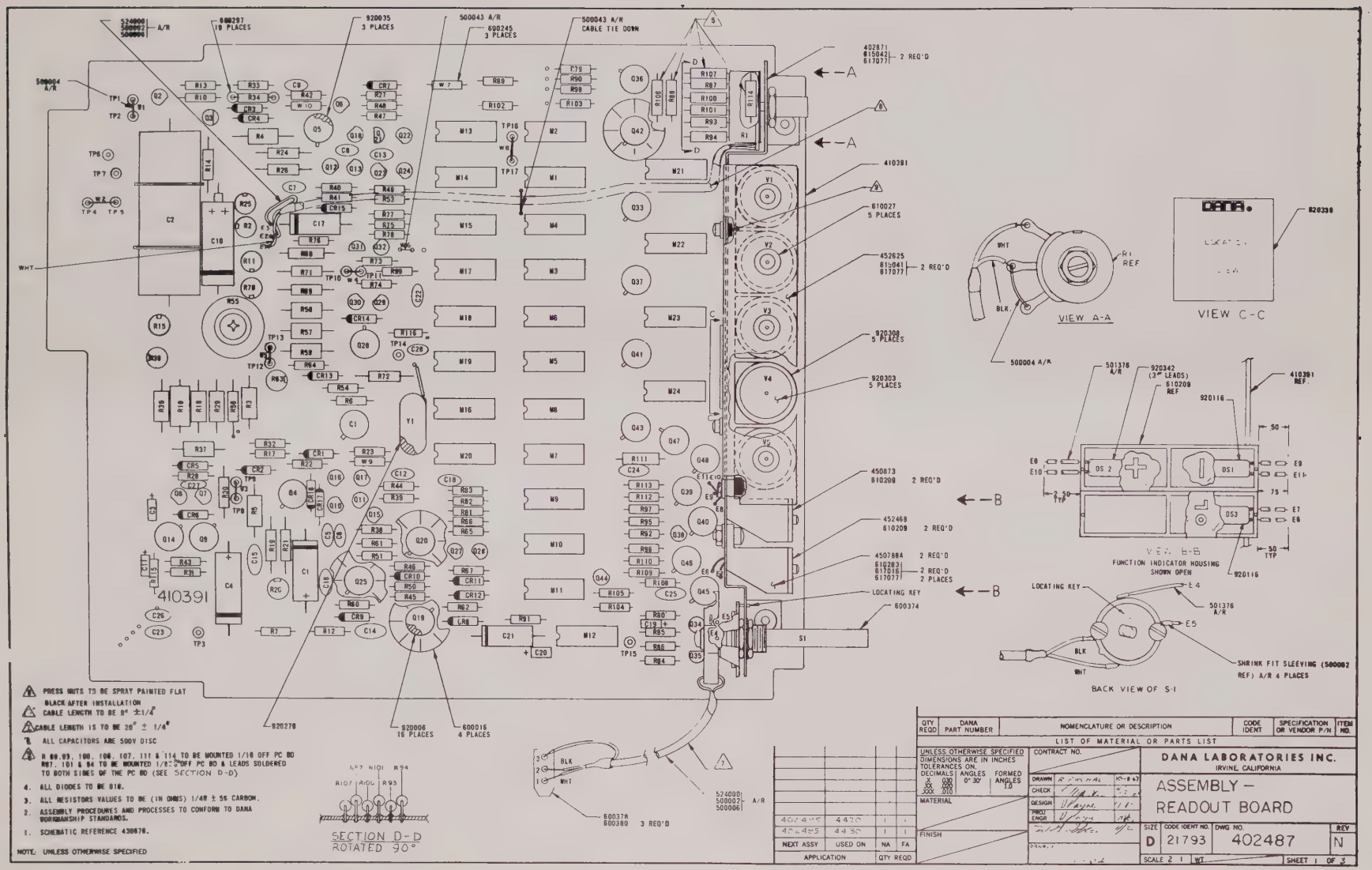
(c) Adjust R15 for a display reading of -1.0000.

SECTION 6

DRAWINGS

6.1 DRAWINGS

Readout Assembly	402487
Readout Assembly	430676
Power Supply Assembly, 4430	402488
Power Supply Assembly, 4470	402497
PCB Assembly - Power Supply, 4470	402498
Power Supply Schematic	430677
PCB Assembly - Power Supply, 4430	402489
Assembly, 212 Module	402567
PCB Assembly, 212	402559
PCB Schematic, 212	430708



⚠ PRESS NUTS TO BE SPRAY PAINTED FLAT BLACK AFTER INSTALLATION

⚠ CABLE LENGTH IS TO BE 8" ±1/4"

⚠ CABLE LENGTH IS TO BE 20" ± 1/4"

⚠ ALL CAPACITORS ARE 500V DISC

⚠ R 89,93, 100, 106, 107, 111 & 114 TO BE MOUNTED 1/16 OFF PC BD R87, 101 & 84 TO BE MOUNTED 1/8 OFF PC BD & LEADS SOLDERED TO BOTH SIDES OF THE PC BD (SEE SECTION D-D)

4. ALL DIODES TO BE 018.
3. ALL RESISTORS VALUES TO BE (IN OHMS) 1/4W ± 5% CARBON.
2. ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS.
1. SCHEMATIC REFERENCE 430678.

NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
402485	4470	1			
402485	4430	1	1		
NEXT ASSY	USED ON	NA	FA		
APPLICATION		QTY REQD			

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS | ANGLES | FORMED ANGLES
X .XX .XXX | 0° 30' | 1.0

MATERIAL

FINISH

CONTRACT NO.

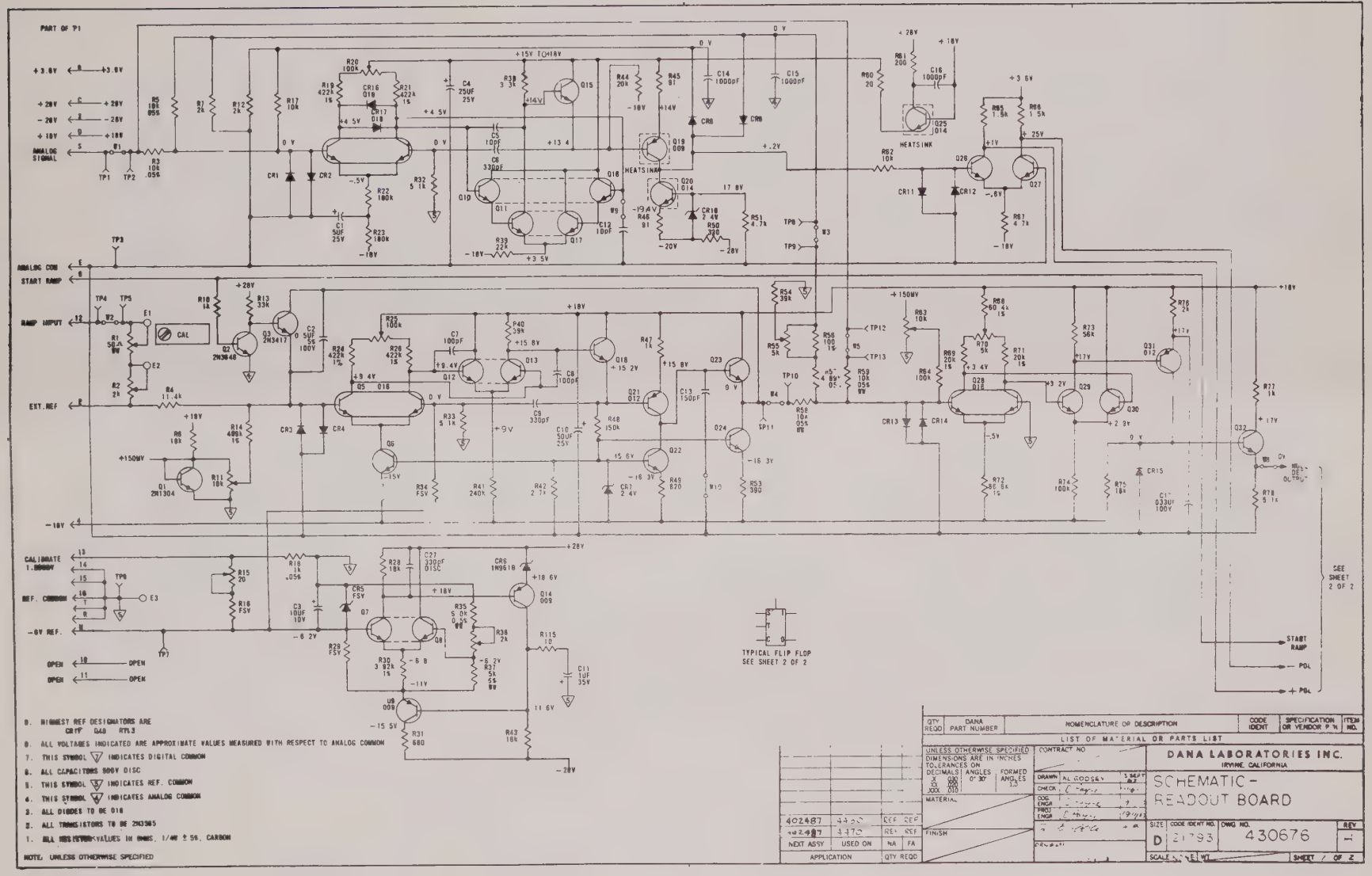
DRAWN	R. PARKHAM	10-8-67
CHECK		
DESIGN		
PROJ ENGR		
DEPT.		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

ASSEMBLY — READOUT BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402487	N

SCALE 2 : 1 | WT. | SHEET 1 OF 3



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
LIST OF MATERIAL OR PARTS LIST					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS: X .030, XX .010, XXX .010; ANGLES 0° 30'; FORMED ANGLES 1.5

MATERIAL

FINISH

402487	4420	REF DES	REF DES
402487	4370	REF DES	REF DES
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

CONTRACT NO

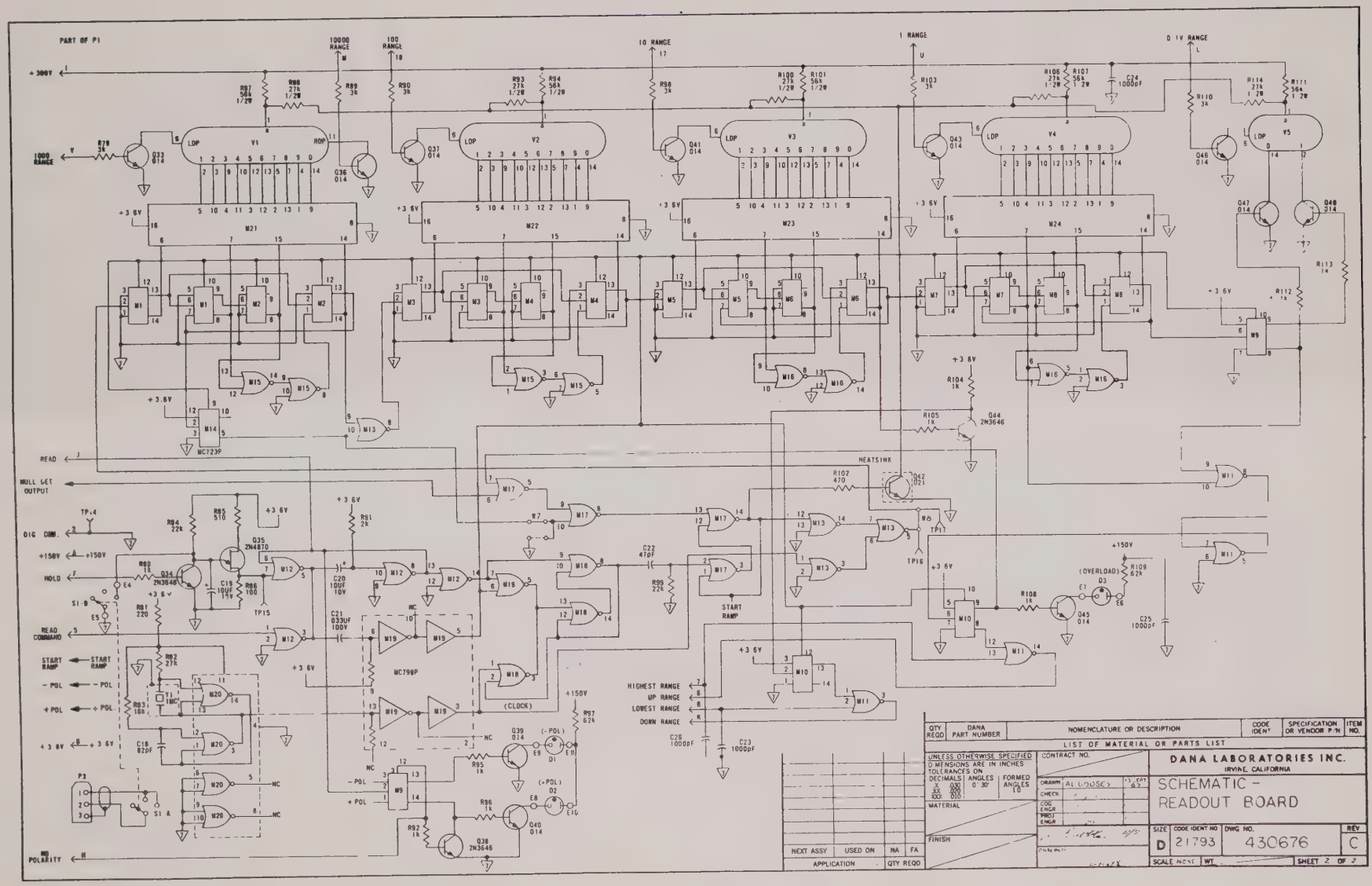
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN	AL GOOSEY	3 SEPT 67
CHECK		
DOC ENGR		
PROJ ENGR		

SCHEMATIC - READOUT BOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	430676	1

SCALE | WT | SHEET 1 OF 2



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS: XX .010, XXX .010 | ANGLES 0° 30' | FORMED ANGLES 10

CONTRACT NO.

DRAWN: AL COOSEY

CHECK

ENGR

MATERIAL

FINISH

NEXT ASSY | USED ON | NA | FA

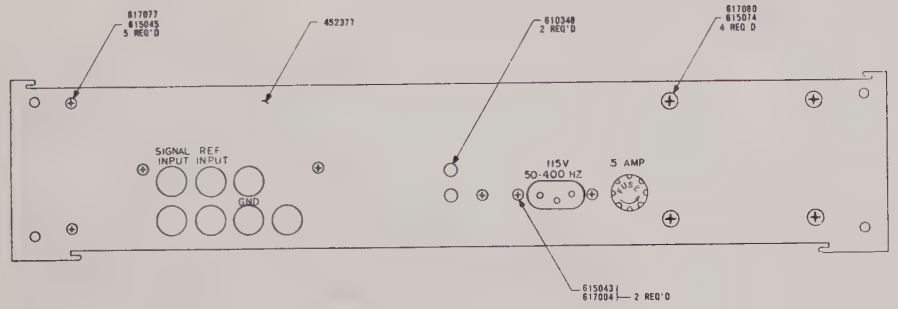
APPLICATION | QTY REQD

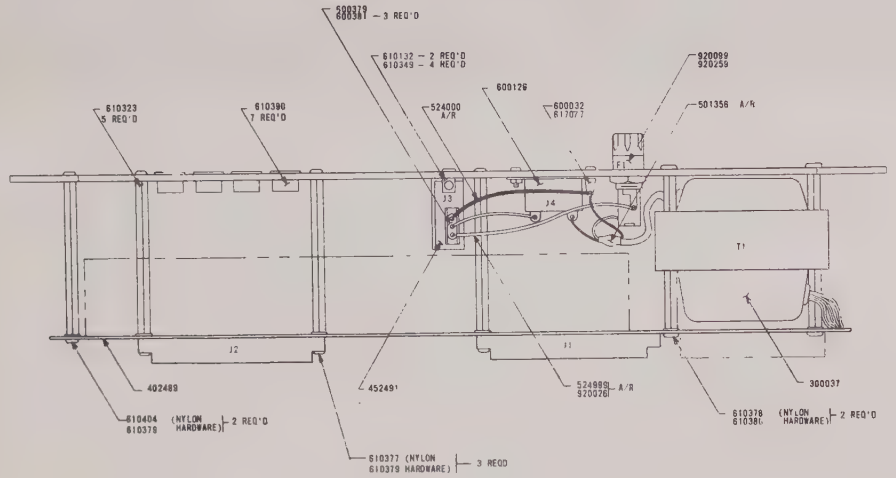
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC - READOUT BOARD

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	430676	C

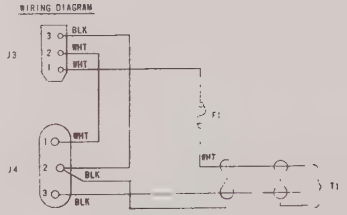
SCALE NONE | WT. | SHEET 2 OF 2





WIRE LIST			
402489	E#	COLOR	T1
	2	GY	
	9	BLU	
	3	VIO	
	4	BRN	
	8	GRN	
	6	ORG	
	7	YEL	
	10	BLK	
	5	RED	
402489	1	WHT	T1

WIRING DIAGRAM



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			
402485	4430	1 1			
NEXT ASSY	USED ON	NA FA			
APPLICATION		QTY REQD			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS: X .030, XX .020, XXX .010 / ANGLES 0° 30' / FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN	AL GODSEY	FEB 1969
CHECK	J. ENGLISH	10-69
DESIGN	D.L.	
PROJ ENGR	M.A.	

POWER SUPPLY ASSY
FULL RACK

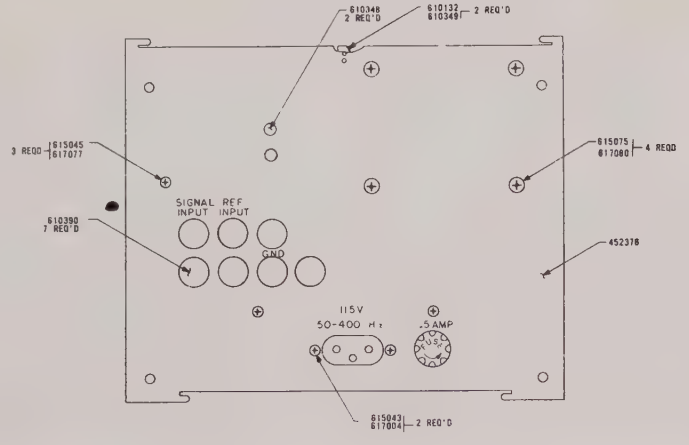
SIZE	CODE IDENT NO.	DWG NO	REV
D	21793	402488	D

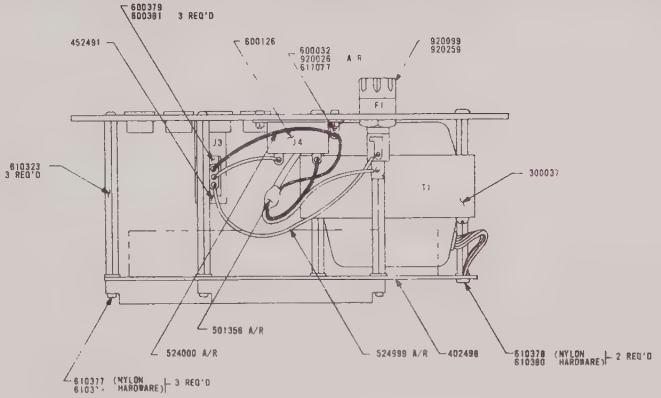
SCALE 1 / 1 WT SHEET 1 OF 1

2. SCHEMATIC REF. NO 430877

1 ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM WITH DANA WORKMANSHIP STANDARDS

NOTE: UNLESS OTHERWISE SPECIFIED





WIRE LIST			
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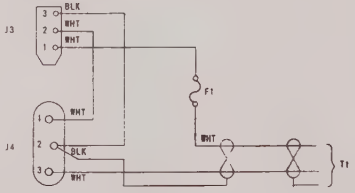
	9	BLU	
	7	YEL	
	10	BLK	
	3	VIO	
	1	WHT	
	2	GY	
	8	ORG	
	4	BRN	
402498	6	GRN	T1

WIRING DIAGRAM



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			
402590	4470				
402495	4470				
NEXT ASSY	USED ON	NA	FA		
APPLICATION		QTY REQD			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS: .XX ±.030, .XXX ±.010
ANGLES ± 0° 30'
FORMED ANGLES ±.0
MATERIAL
FINISH

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE CALIFORNIA

DRAWN	AL GOOSEY	3 OCT 1967
CHECK	U. LOVELESS	10-25-67
DESIGN	U.L.	10-25-67
PROJ ENGR	[illegible]	10/26/67

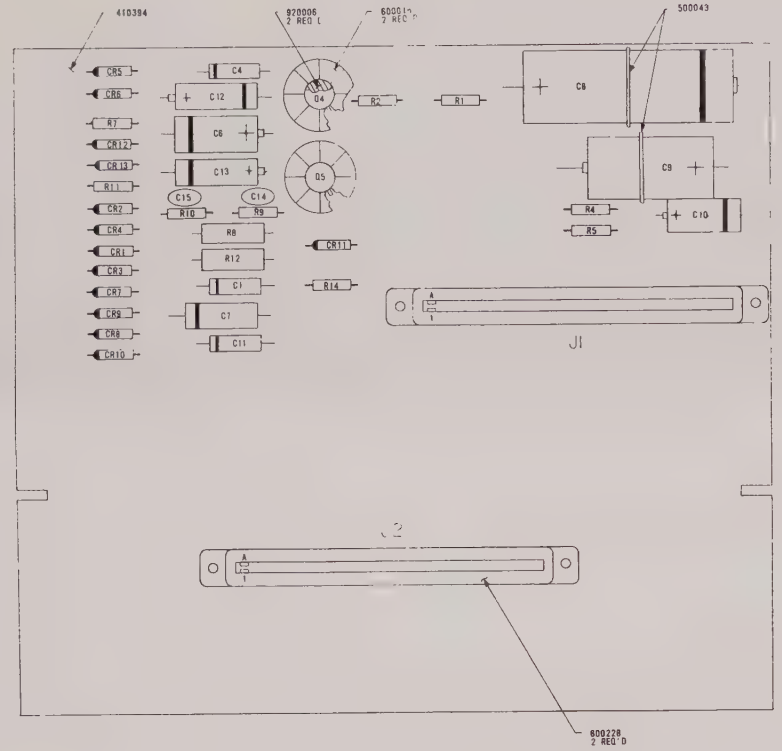
POWER SUPPLY ASSY - HALF RACK

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	402497	C

SCALE 1 / 1 | WT | SHEET 1 OF 1

2. SCHEMATIC REF. NO 430677
1. ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM WITH DANA WORKMANSHIP STANDARDS

NOTE. UNLESS OTHERWISE SPECIFIED



P/N	DESCRIPTION	QTY
410384	PCB-PWR SUP	1
452485	INSULATOR-MYLAR	1
500002	SHRINK TUBING	A/R
500006	CABLE-SHLD	A/R
500018	TEFLON TUBING	A/R
500043	BUSS WIRE, TEFLON	A/R
600018	HEAT SINK	2
600228	CONNECTOR	2
600273	HEAT SINK	1
810345	RIVET-SEMI TUB 3 16	4
815043	SCREW-PPH 4-40	2
817004	HEX NUT 4-40	2
817077	LOCKWASHER #4	2
920008	TRANSISTOR PAD-LG	3
920010	SOLDER-BAR	A/R
920026	SOLDER-WIRE	A/R
920287	COMPONENT CLIP	2

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P N	ITEM NO

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS X .06, XX .020, XXX .010; ANGLES 0° 30'; FORMED ANGLES 1°

MATERIAL

FINISH

CONTRACT NO

DRAWN

CHECK

DESIGN

PROJ ENGR

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY-POWER SUPPLY INTERCONN HALF RACK

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	402498	C

SCALE 2/1 WT SHEET OF

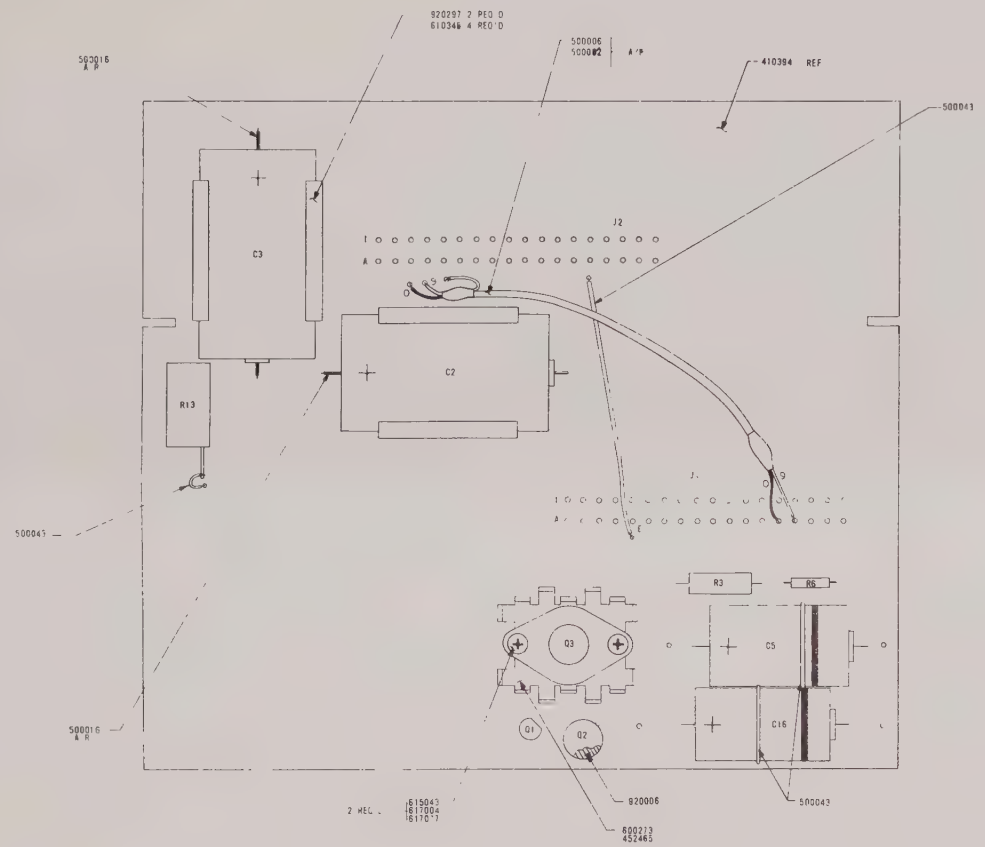
402497	4470	1	
NEXT ASSY	USED ON	NA	NA
APPLICATION		QTY REQD	

3 SCHEMATIC REF 430677

2 ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS

1 ALL RESISTORS ARE 1/4W 5%, CARBON

NOTE UNLESS OTHERWISE SPECIFIED



REF DES	PART NO	DESCRIPTION
CR13	220015	IN967 B
CR12	220015	IN967 B
CR11	221177	1 4M2 4AZ5
CR10	210004	SD4
CR9	210004	SD4
C16	110018	1000UF 15V
C15	101174	001UF 500V
C14	101174	001UF 500V
C13	110043	250F 25V
C12	110043	250F 25V
C11	121088	01UF 100V
C10	110083	100UF 12V
C9	110066	15UF 200V
C8	110065	20UF 350V
C7	120072	01UF 600V
C6	110083	100UF 12V
C5	110065	2000UF 10V
C4	121088	01UF 100V
C3	110067	2000UF 35V
C2	110067	2000UF 35V
C1	121088	01UF 100V

REF DES	PART NO	DESCRIPTION
R14	000511	51Ω
R13	040063	500 CTS
R12	030007	150 3W WW
R11	000202	2k
R10	000151	150
R9	000151	150
R8	030007	150 3W WW
R7	000202	2k
R6	000224	220k
R5	000751	750
R4	000751	750
R3	030014	220k 1W
R2	000241	240
R1	00024	240
Q5	200[illegible]	009
Q4	200035	014
Q3	200030	RCA40250
Q2	200035	014
Q1	200043	2N3565

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P N	ITEM NO
		LIST OF MATERIAL OR PARTS LIST			

402497		1	1
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS ANGLES FORMED
X .030 0 30' ANGLES
XX .010 1.0
XXX .010

MATERIAL

FINISH

CONTRACT NO.

DRAWN A. [illegible]

CHECK [illegible]

DESIGN [illegible]

PROJ ENGR [illegible]

ENGR

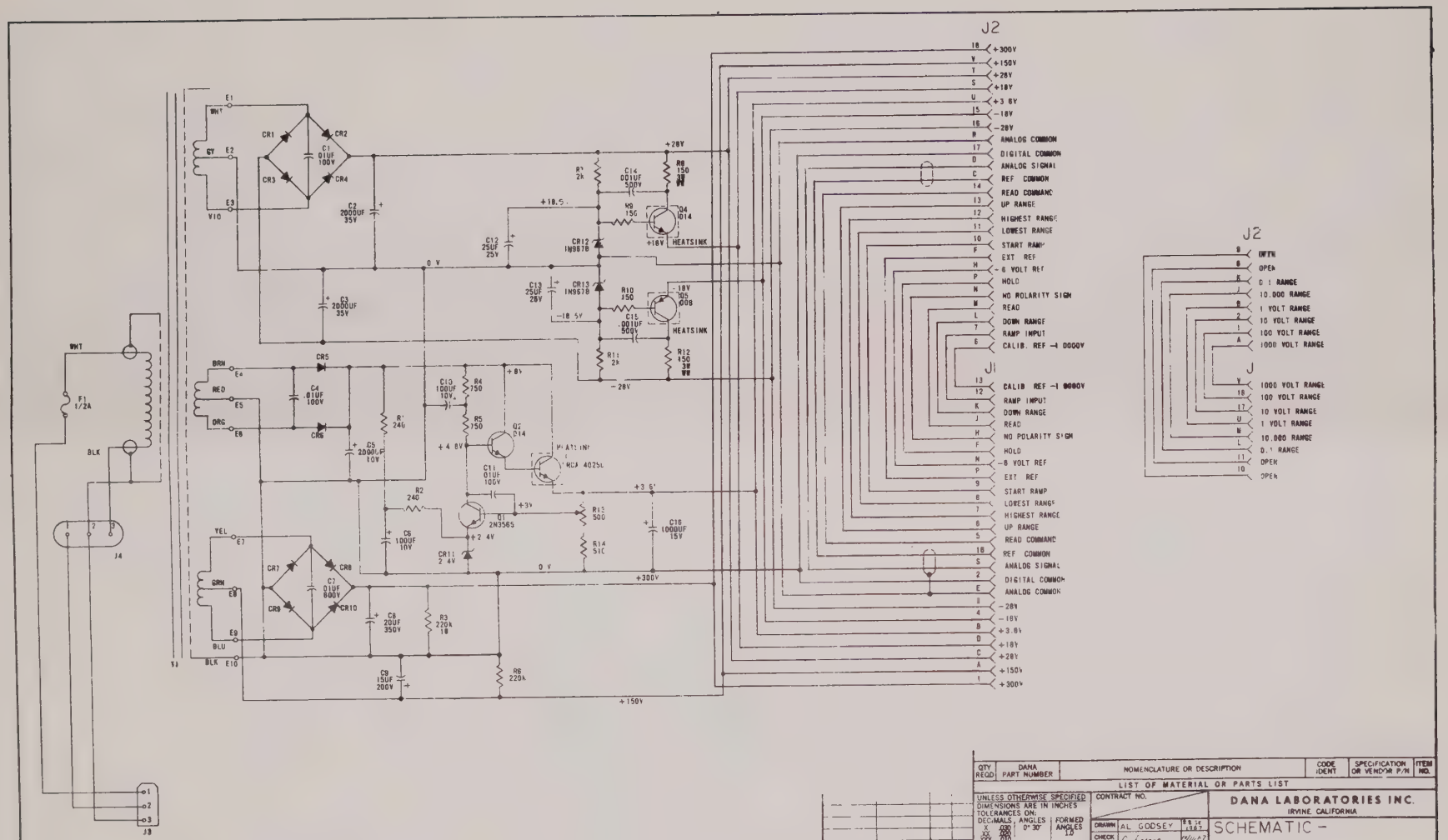
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PCB ASSY POWER SUPPLY / INTERCOM. HALF RACK

SIZE	IDENT NO	DWG NO	REV
D	21793	402498	C

SCALE 1 WT SHEET 1 OF 2

NOTE UNLESS OTHERWISE SPECIFIED



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
402497	4470	REF	REF		
402498	4430	REF	REF		
NEXT ASSY	USED ON	NA	FA		
APPLICATION		QTY REQD			

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS ANGLES FORMED ANGLES
X .000 0° 30' 1/2
XX .000
XXX .010

MATERIAL

FINISH

CONTRACT NO.

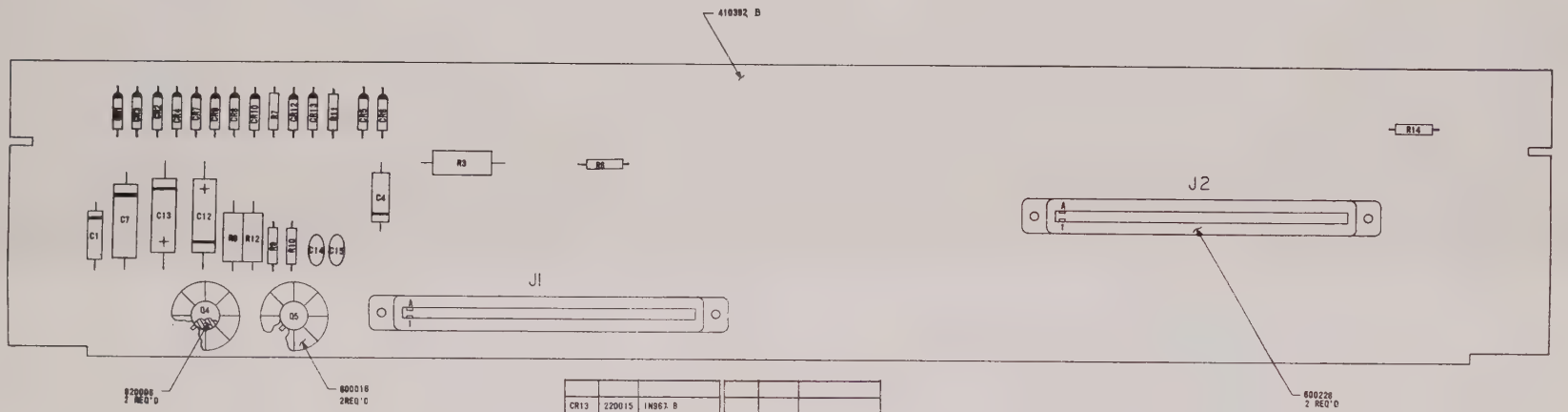
DRAWN	AL GODSEY	8 & 14 1965
CHECK		
DSG ENGR		
PROJ ENGR		

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

SCHEMATIC - POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	430677	B

SCALE NONE WT SHEET 1 OF 1



REF DES	PART NO	DESCRIPTION
CR13	220015	IN967 B
CR12	220015	IN967 B
CR11	221177	1/4W2.4AZ5
CR10	210084	SD4
CR1	210004	SD4
C16	110018	1000UF/15V
C15	101174	.001UF/500V
C14	101174	.001UF/500V
C13	110043	25UF/25V
C12	110043	25UF/25V
C11	121088	.01UF/100V
C10	110083	100UF/12V
C9	110066	15UF/200V
C8	110065	20UF/350V
C7	120072	.01UF/600V
C6	110083	100UF/12V
C5	110065	2000UF/10V
C4	121088	.01UF/100V
C3	110067	2000UF/35V
C2	110087	2000UF/35V
C1	121088	.01UF/100V

REF DES	PART NO	DESCRIPTION
R14	000511	510Ω
R13	040063	500Ω/CTS
R12	030007	150Ω/3W/WW
R11	000202	2k
R10	000151	150Ω
R9	000151	150Ω
R8	030007	150Ω 3W/WW
R7	000202	2k
R6	000224	220k
R5	000751	750Ω
R4	000751	750Ω
R3	030014	220k/1W
R2	000241	240Ω
R1	000241	240Ω
Q5	200011	009
Q4	200035	014
Q3	200030	RCA40250
Q2	200035	014
Q1	200043	2N3585

402488	4430	J	J
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX ±.030, .XXX ±.010; ANGLES 0° 30'; FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN	AL GODSEY	8 SEPT 1967
CHECK		
DESIGN	D Payne	10/16/67
PROJ ENGR	D Payne	10/16/67
		11/2

PCB ASSY-POWER SUPPLY/INTERCONN

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402489	C

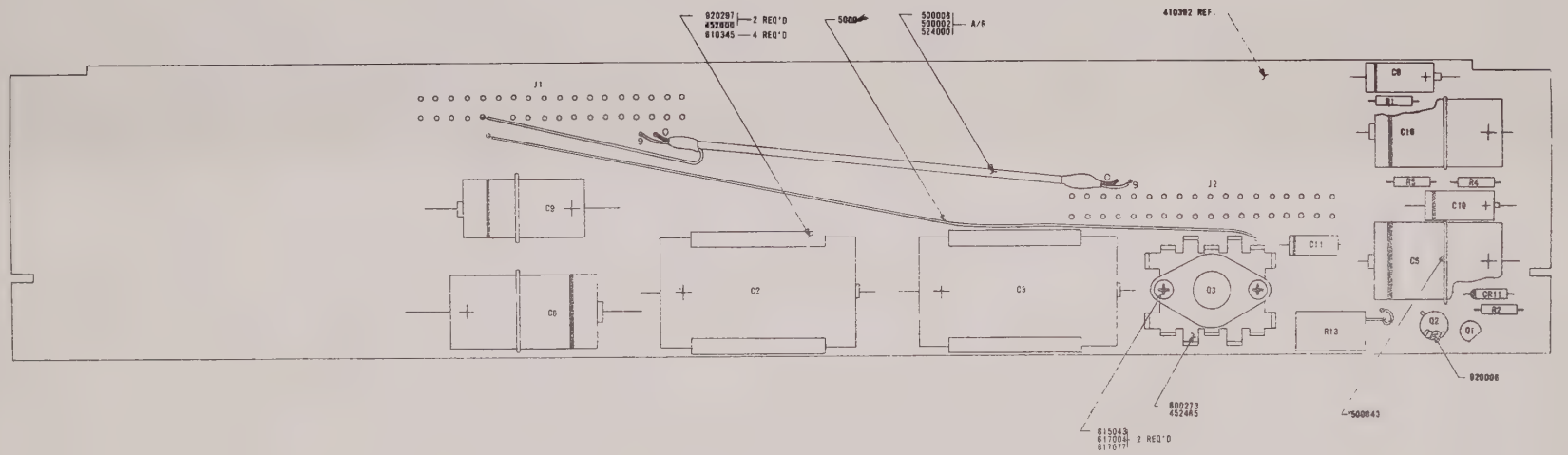
SCALE 2/1 WT SHEET 1 OF 2

3 SCHEMATIC REFERENCE: 430077

2 ASSEMBLY PROCESSES AND PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

1 ALL RESISTORS TO BE 1/4W, 5%, CARBON

NOTE: UNLESS OTHERWISE SPECIFIED



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: X .030, XX .010, XXX .005 | ANGLES 0° 30' | FORMED ANGLES 1.0

CONTRACT NO

DRAWN AL GODSEY 10 SEPT 1981

CHECK 10-7-81

DESIGN 10/7/81

PROJ ENGR 10/7/81

MATERIAL

FINISH

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

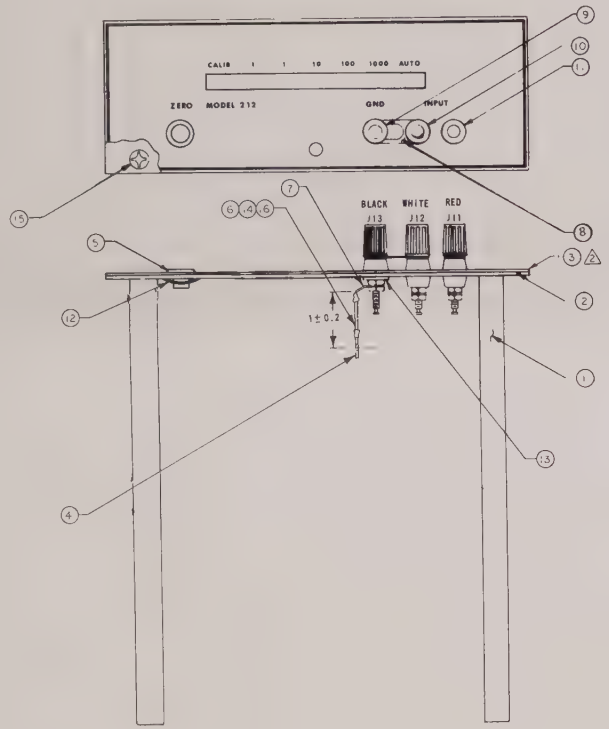
PCB ASSY - POWER SUPPLY/INTERCONN

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402489	C

SCALE 2/1 WT SHEET 2 OF 2

402488	4430	1	1
NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

NOTE: UNLESS OTHERWISE SPECIFIED



REF DES OR ITEM	P/N	DESCRIPTION	QTY
1	452474	SIDE-CONT. MODULE	2
	452372	EXTRUSION	REF
2	452528	PANEL-FRONT, MODULE	1
3	452530	PANEL-FRONT SS	1
	452529	PANEL-FRONT, COVER	REF
4	452601	CLIP-SPRING TENSION	1
5	452783	BUSHING-PANEL	1
6	501355	TUBING-SHRINK FIT .07 ID	A/R
7	800022	LUG-SOLDER	1
8	800239	SHORTING LINK	1
9	800330	BINDING POST-BLACK	1
10	800331	BINDING POST-WHITE	1
11	800332	BINDING POST-RED	1
12	810326	CLIP-SHAFT 3/8 DIA.	1
13	817103	WASHER-FLAT	1
14	524000	WIRE-24 GA STR 0 COLOR	A/R
15	818082	SCREW TAPPING PFH 8-32 X 1/2	4
16	820028	SOLDER-WIRE 0.03263 /37 RESIN CORE	A/R

402 568	212 / STD	1	1
402 577	212/REAR INP	1	1
NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS: X .030, XX .020, XXX .010
ANGLES: 0° 30', FORMED 1° 0'
HOLE DIAMETERS: =.004, .001
MATERIAL
FINISH

DRAWN	Al Godsey	25 APR 63
CHECK	P.F. Conover	9-14-61
DESIGN	P.F. Conover	9-14-61
MECH ENGR	Wasa	9/6/63
PROJ ENGR	D. Pierpont	9/6/63

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

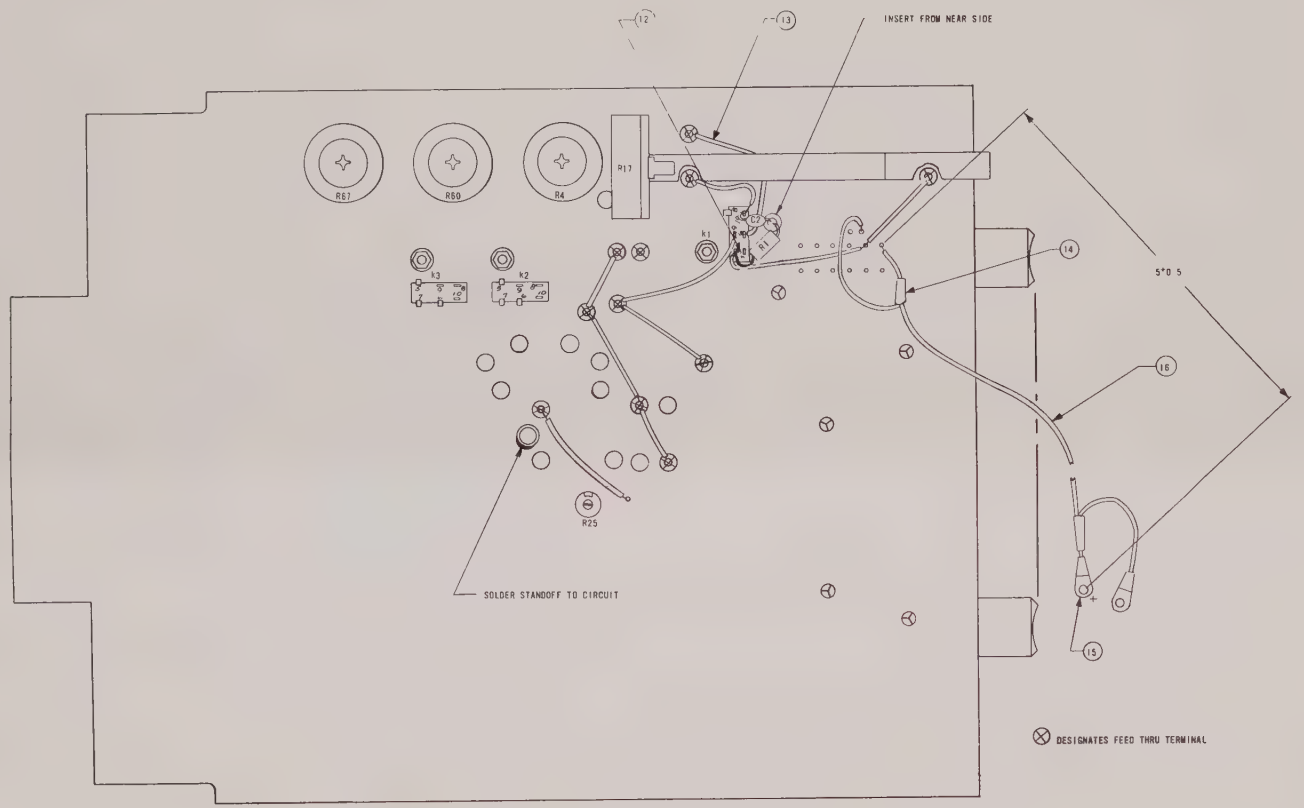
ASSEMBLY MODULE
CHASSIS

SIZE	CODE IDENT NO	DWG NO	REV
D	21793	402567	

SCALE 1/1 SHEET 1 OF 1

⚠2 USING EXISTING ADHESIVE ON COVER, BOND FRONT COVER TO FRONT PANEL.
1 ASSEMBLY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES UNLESS OTHERWISE SPECIFIED



6 Q14 & Q16 ARE MATCHED SET

7 Q8 & Q9 ARE MATCHED SET

8 Q6, Q7 AND Q14, Q16 BONDED TOGETHER, AS SHOWN, WITH EASTMAN 910. P/N 820008

5 SCHEMATIC REFERENCE: 430708

4 ALL ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS

3 INSERT TEFLON TERMINALS FROM FARSIDE

2 ALL RESISTOR VALUES ARE IN OHMS

1 ALL RESISTORS ARE 1/4 W, ±5%, CARBON

NOTE: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	NA	FA
	212	1	1
APPLICATION		QTY REQD	

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS X .030 .XX .010 | ANGLES 0° 30' | FORMED ANGLES TO

MATERIAL

FINISH

CONTRACT NO.

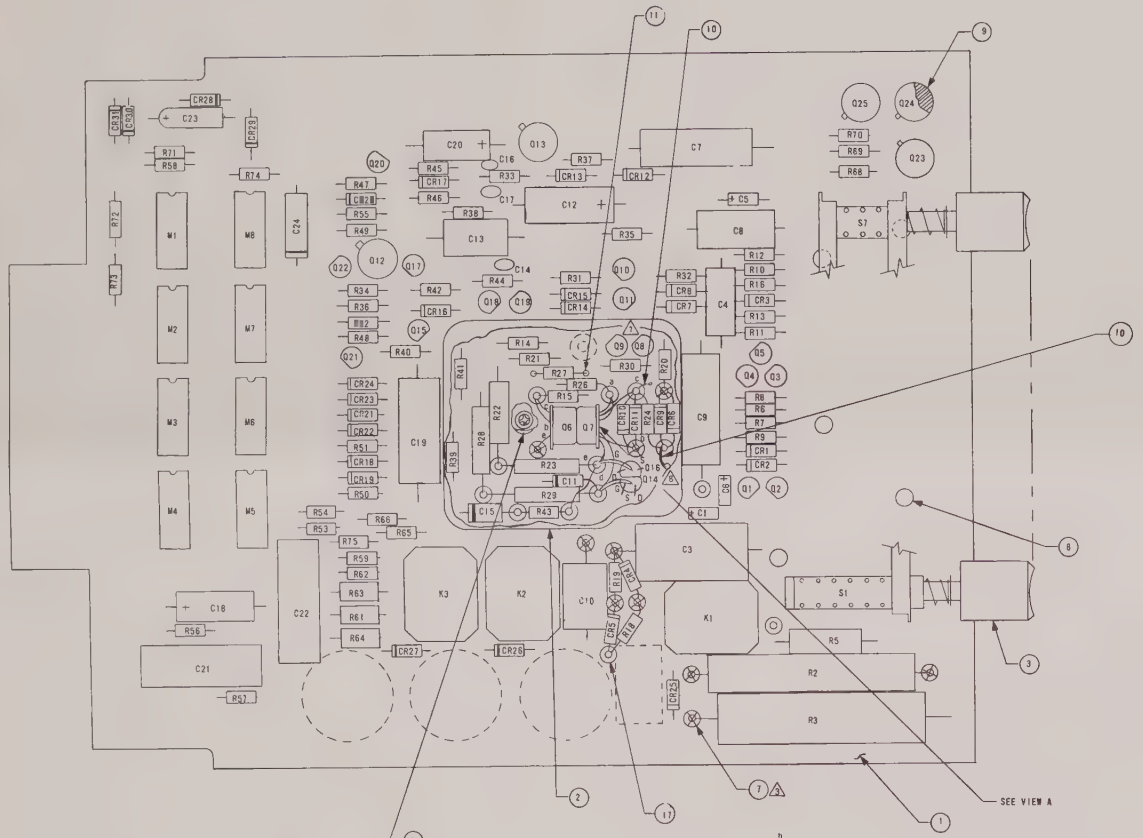
DRAWN Jim Antista 3-6-68
CHECK [illegible] 3/6/68
DESIGN [illegible] 3/6/68
PROJ ENGR [illegible] 3/6/68

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P C BOARD ASSEMBLY MILLIVOLT ISOLATOR (212)

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402559	D

SCALE 2/1 | WT | SHEET 1 OF 5



SEE SHEET 1 OF 5

NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX ±.02, .XXX ±.010; ANGLES 0° 30'; FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

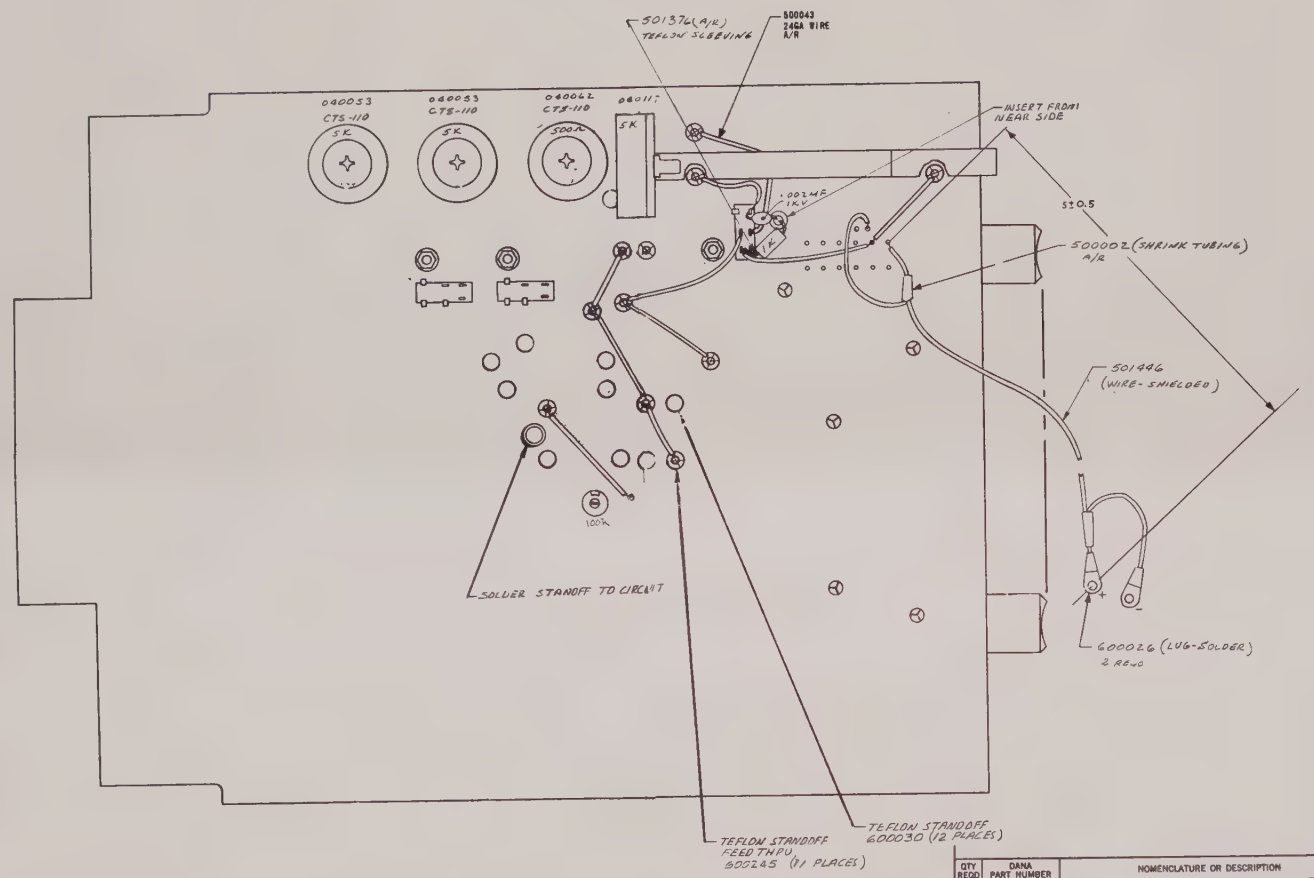
DRAWN	P Nielsen	7-25-68
CHECK	[illegible]	8/1/68
DESIGN	Wuee	8/1/68
PROJ ENGR	[illegible]	7/25/68
DRAWING	D Phipps 5/3/68	

ASSEMBLY 212
MILLIVOLT ISOLATOR

NEXT ASSY	USED ON	NA	FA
	212		
APPLICATION		QTY REQD	

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402559	D

SCALE 2 | WT | SHEET 2 OF 2



⚠ Q6, Q7 AND Q14, Q18 BONDED TOGETHER, AS SHOWN WITH EASTMAN 910. P/N 820008

5 SCHEMATIC REFERENCE 430708

4 ALL ASSEMBLY PROCEDURES AND PROCESSES TO CONFORM TO DANA WORKMANSHIP STANDARDS

⚠ INSERT TEFLON TERMINALS FROM FARSIDE

2 ALL RESISTOR VALUES ARE IN OHMS

1 ALL RESISTORS ARE 1/4 W. ±5%. CARBON

NOTE: UNLESS OTHERWISE SPECIFIED

NEXT ASSY	USED ON	NA	FA
APPLICATION		QTY REQD	

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX ±.02, .XXX ±.010; ANGLES 0° 30'; FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO.

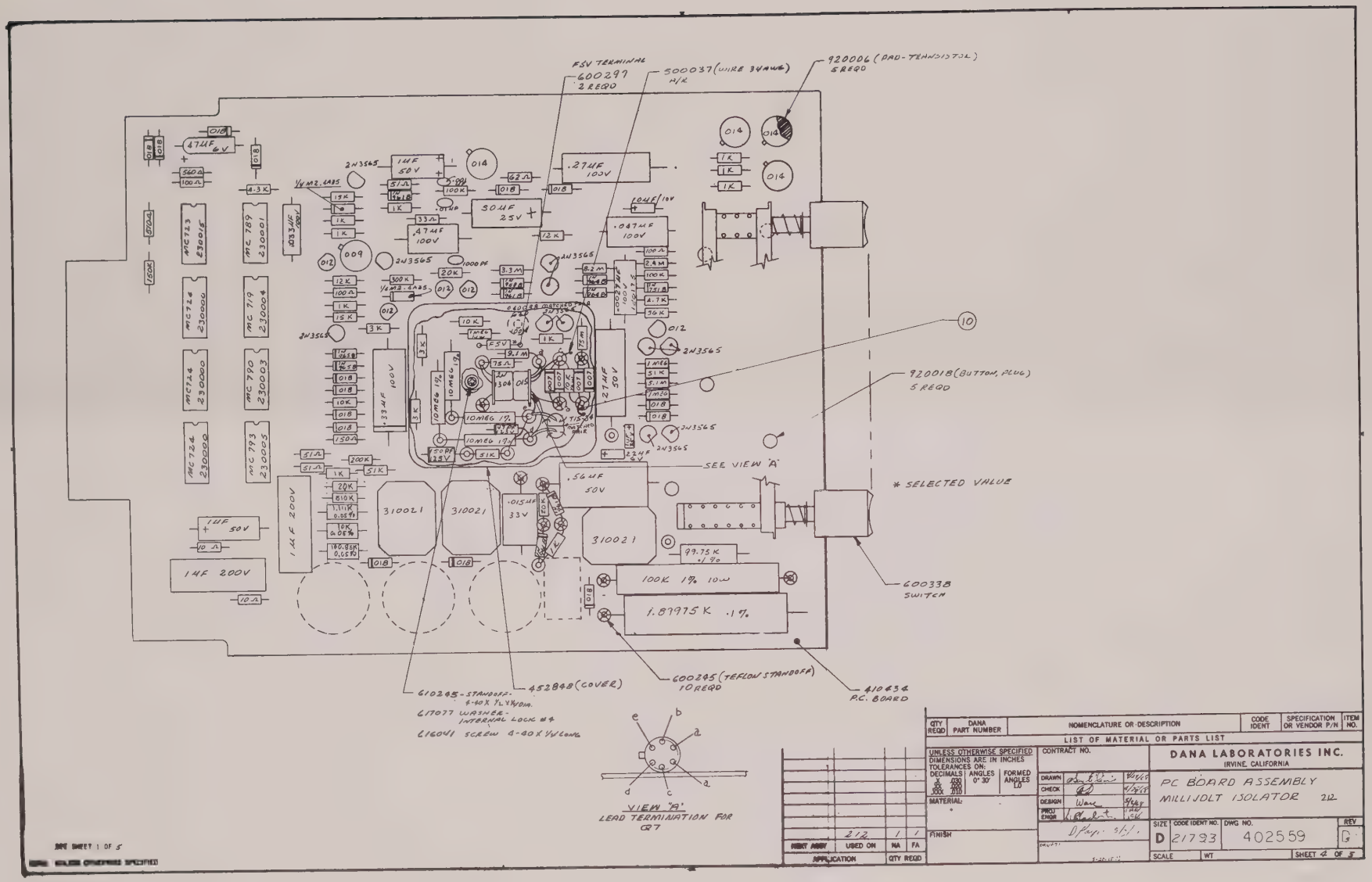
DRAWN	Jim Coates	3-6-68
CHECK		3/6/68
DESIGN		3/6/68
PROJ ENGR		3/6/68

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

P C BOARD ASSEMBLY MILLIVOLT ISOLATOR (213)

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402559	C

SCALE 2/1 WT SHEET 2 OF 5



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS .XXX ±.005, .XX ±.010; ANGLES 0° 30'; FORMED ANGLES ±0
MATERIAL:
FINISH

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN	[illegible]	4/15/68
CHECK	[illegible]	4/15/68
DESIGN	Ware	4/15/68
PROJ ENGR	[illegible]	4/15/68

PC BOARD ASSEMBLY
MILLIVOLT ISOLATOR 212

NEXT ASSY	USED ON	NA	FA
	212	/	/
APPLICATION		QTY REQD	

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	402559	G

SCALE | WT | SHEET 2 OF 5

SHEET 1 OF 5

REF DES OR ITEM	P/N	DESCRIPTION	QTY
C1	110070	22UF/6V	1
C2	100022	.002 UF/1KV DISC	1
C3	120177	.56UF/50V	1
C4	120175	.0027UF/100V	1
C5	110069	10UF/10V	1
C6	110071	1UF/35V	1
C7	120113	.27UF/100V	1
C8	121093	.047UF/100V	1
C9	120178	.27UF/50V	1
C10	120135	.015UF/33V	1
C11	120153	47PF/125V	1
C12	110047	50UF/25V	1
C13	120026	.47UF/100V	1
C14	101174	1000PF DISC	2
C15	120176	150PF/63V	1
C16	101174	1000PF DISC	REF
C17	100017	.01UF/200V DISC	1
C18	110040	1UF/50V	2
C19	120135	.33UF/100V	1
C20	110040	1UF/50V	REF
C21	120134	1UF/200V	2
C22	120134	1UF/200V	REF
C23	110086	47UF/6V	1
C24	121091	.033UF/100V	1

REF DES OR ITEM	P/N	DESCRIPTION	QTY
CR25	211083	018	REF
CR26	211083	018	REF
CR27	211083	018	REF
CR28	211083	018	REF
CR29	211083	018	REF
CR30	211083	018	REF
CR31	211083	018	REF
K1	310029	RELAY	1
K2	310021	RELAY	2
K3	310021	RELAY	REF
M1	230015	MC723	1
M2	230000	MC724	3
M3	230000	MC724	REF
M4	230000	MC724	REF
M5	230005	MC793	1
M6	230003	MC790	1
M7	230094	MC719	1
M8	230001	MC789	1
Q1	200043	2N3565	9
Q2	200043	2N3565	REF
Q3	200043	2N3565	REF
Q4	200043	2N3565	REF

REF DES OR ITEM	P/N	DESCRIPTION	QTY
R4	040062	POT-500CTS-100	1
R5	010334	99.75K 1%	REF
R6	000513	51K 1/4W 5%	3
R7	000515	5.1 MEG 1/4 W 5%	1
R8	000105	1 MEG 1/4W 5%	3
R9	000105	1 MEG 1/4W 5%	REF
R10	000245	2.4 Meg 1/4W 5%	1
R11	000563	56K 1/4W 5%	1
R12	000101	100 1/4W 5%	3
R13	000472	4.7K 1/4W 5%	1
R14	000103	10K 1/4W 5%	3
R15	000750	75 1/4W 5%	1
R16	000104	100K 1/4W 5%	2
R17	040117	POT 5K CTS	1
R18	000102	1K 1/4W 5%	REF
R19	000203	20K 1/4W 5%	3
R20	000756	75M 1/4W 5%	1
R21	000105	1M 1/4W 5%	REF
R22	010337	10M 1%	4
R23	010337	10M 1%	REF
R24	000103	10K 1/4W 5%	REF
R25	040088	POT 100K 62P	1
R26	000916	9.1M 1/4W 5%	1
R27	001734	FSV	1
R28	010337	10M 1%	REF

REF DES OR ITEM	P/N	DESCRIPTION	QTY
R54	000510	51 1/4W 5%	REF
R55	000102	1K 1/4W 5%	REF
R56	000100	10 1/4W 5%	2
R57	000100	10 1/4W 5%	REF
R58	000101	100 1/4W 5%	REF
R59	000203	20K 1/4W 5%	REF
R60	040053	POT 5K CTS-110	2
R61	020241	10K .05%	1
R62	000514	510K 1/4W 5%	1
R63	020204	1.111K .05%	1
R64	020170	100.83 .05%	1
R65	000513	51K 1/4W 5%	REF
R66	000204	200K 1/4W 5%	1
R67	040053	POT 5K CTS-110	REF
R68	000102	1K 1/4W 5%	REF
R69	000102	1K 1/4W 5%	REF
R70	000102	1K 1/4W 5%	REF
R71	000561	560 1/4W 5%	1
R72	000511	510 1/4W 5%	1
R73	000154	150K 1/4W 5%	1
R74	000432	4.3K 1/4W 5%	1
R75	000102	1K 1/4W 5%	REF
1	410434B	PCB CONTRL M.V.	1
2	452348	COV. ENVIR. SHIELD	1

REF DES OR ITEM	P/N	DESCRIPTION	QTY
CR1	211083	018	15
CR2	211083	018	REF
CR3	220007	1N751B	1
CR4	220004	1N961B	4
CR5	220004	1N961B	REF
CR6	211236	007	4
CR7	220016	1N964B	2
CR8	220016	1N964B	REF
CR9	211236	007	REF
CR10	211236	007	REF
CR11	211236	007	REF
CR12	211083	018	REF
CR13	211083	018	REF
CR14	220004	1N961B	REF
CR15	220012	1N958B	1
CR16	220030	1/4W 2.4AZ5	2
CR17	220004	1N961B	REF
CR18	211083	018	REF
CR19	211083	018	REF
CR20	220030	1/4W 2.4AZ5	REF
CR21	211083	018	REF
CR22	211083	018	REF
CR23	220022	1N965B	2
CR24	220022	1N965B	REF

REF DES OR ITEM	P/N	DESCRIPTION	QTY
C5	200022	012	5
C6	201084	2N1304	1
C7	200027	015	1
Q8, Q9	200044	2N3565 MATCHED	2
Q10	200043	2N3565	REF
Q11	200043	2N3565	REF
Q12	200052	009	1
Q13	200035	014	4
Q14, Q16	200083	T1534 MATCHED	2
Q15	200022	012	REF
Q17	200043	2N3565	REF
Q18	200022	012	REF
Q19	200022	012	REF
Q20	200043	2N3565	REF
Q21	200043	2N3565	REF
Q22	200022	012	REF
Q23	200035	014	REF
Q24	200035	014	REF
Q25	200035	014	REF
R1	000102	1K 1/4W 5%	11
R2	030015	100K 10W 1%	1
R3	010334	9.89975 K	1

REF DES OR ITEM	P/N	DESCRIPTION	QTY
R29	010337	10M 1%	REF
R30	000102	1K 1/4W 5%	REF
R31	000335	3.3M 1/4W 5%	1
R32	000525	8.2M 1/4W 5%	1
R33	000134	100K 1/4W 5%	REF
R34	000123	12K 1/4W 5%	2
R35	000123	12K 1/4W 5%	REF
R36	000101	100 1/4W 5%	REF
R37	000620	62 1/4W 5%	1
R38	000330	33 1/4W 5%	1
R39	000302	3K 1/4W 5%	3
R40	000302	3K 1/4W 5%	REF
R41	000302	3K 1/4W 5%	REF
R42	000304	300K 1/4W 5%	1
R43	000513	51K 1/4W 5%	REF
R44	000203	20K 1/4W 5%	3
R45	000510	51 1/4W 5%	REF
R46	000102	1K 1/4W 5%	2
R47	000153	15K 1/4W 5%	2
R48	000153	15K 1/4W 5%	REF
R49	000102	1K 1/4W 5%	REF
R50	000151	150 1/4W 5%	1
R51	000103	10K 1/4W 5%	REF
R52	000102	1K 1/4W 5%	REF
R53	000510	51 1/4W 5%	REF

REF DES OR ITEM	P/N	DESCRIPTION	QTY
3	600336	SWITCH M.V. PUSH-BUTTON	1
4	610245	STANDOFF 4-40 X 1/2 X 1/4 DIA	1
5	617077	WASHER-INT. LOC	1
6	616041	SCR 1/4" LG 4-40	1
7	600243	TEFLON FEEDTHRU	11
8	320018	BUTTON FLUS	5
9	320006	TSTR PAD (LG)	5
10	500037	WIRE - 34 AWG	A/R
11	600297	FSV TERMINAL	2
12	501376	TEFLON SLEEVING	A/R
13	500043	WIRE 24 AWG	A/R
14	500002	SHRINK TUBING	A/R
15	600026	LUG SOLDER	2
	430708	SCHEMATIC CON M.V.	REF
16	501446	SHIELDED WIRE	A/R
17	600030	TEFLON STANDOFF	12
18	920010	SOLDER	A/R

NEXT DWG	USED ON	NEXT DWG	FINAL ASSY
	212	1	1
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
DECIMALS: X .030, XX .020, XXX .010
ANGLES: 0° 30' FORMED 1° 0'
HOLE DIAMETERS: +.004 -.001
MATERIAL
FINISH

DRAWN [illegible] 7-3-68
CHECK
DESIGN
MECH ENGR
PROJ ENGR

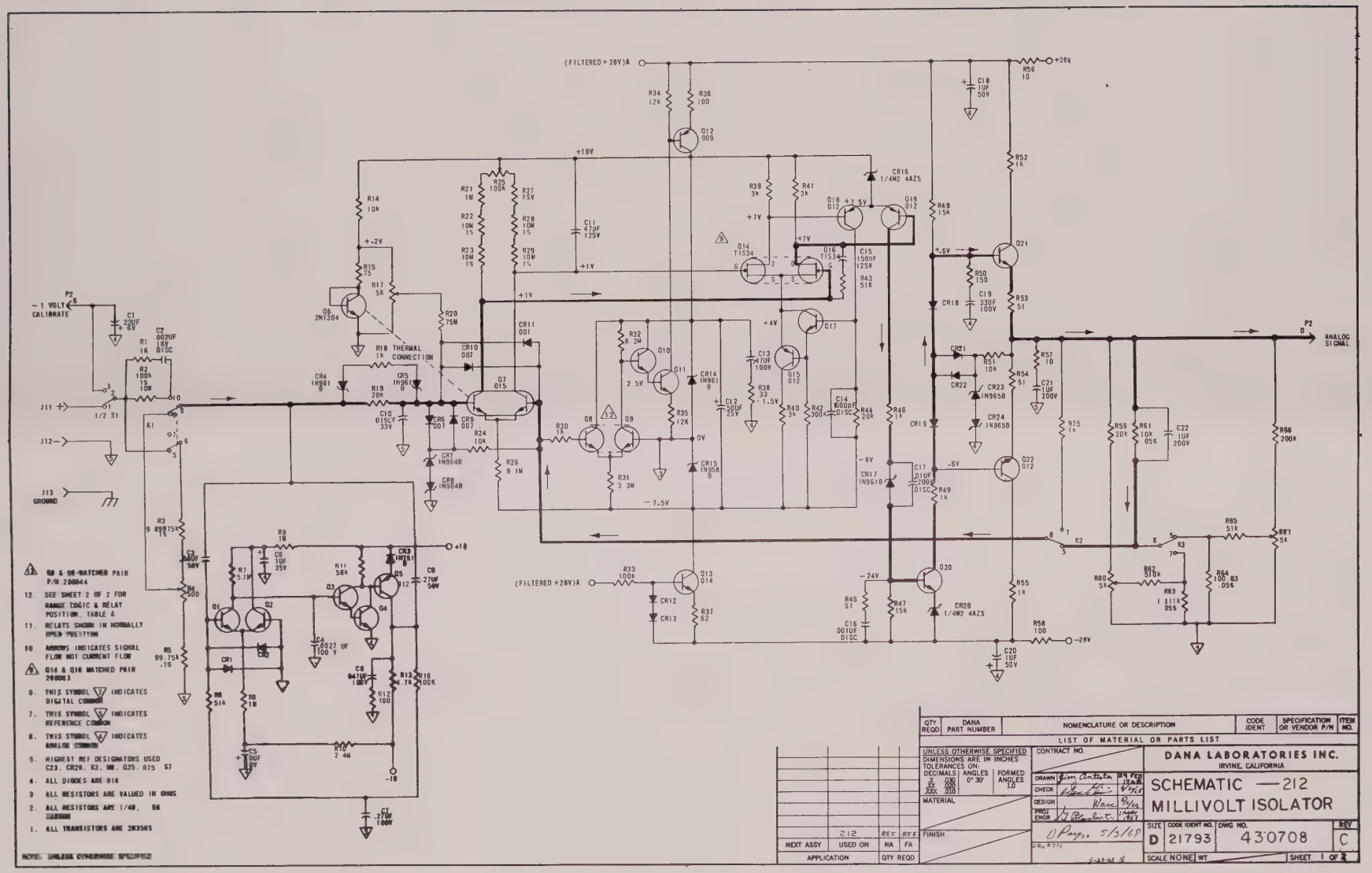
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

PC BOARD ASSEMBLY
MILLIVOLT ISOLATOR 212

SIZE D | CODE IDENT NO. 21793 | DWG NO. 402559 | REV D

SCALE | SHEET 5 OF 5

NOTES UNLESS OTHERWISE SPECIFIED



QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

NEXT ASSY	212	REF	REF
USED ON		NA	FA
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: DECIMALS .X ±.030 .XX ±.020 .XXX ±.010 | ANGLES ± 0° 30' | FORMED ANGLES 1.0
MATERIAL
FINISH

CONTRACT NO.

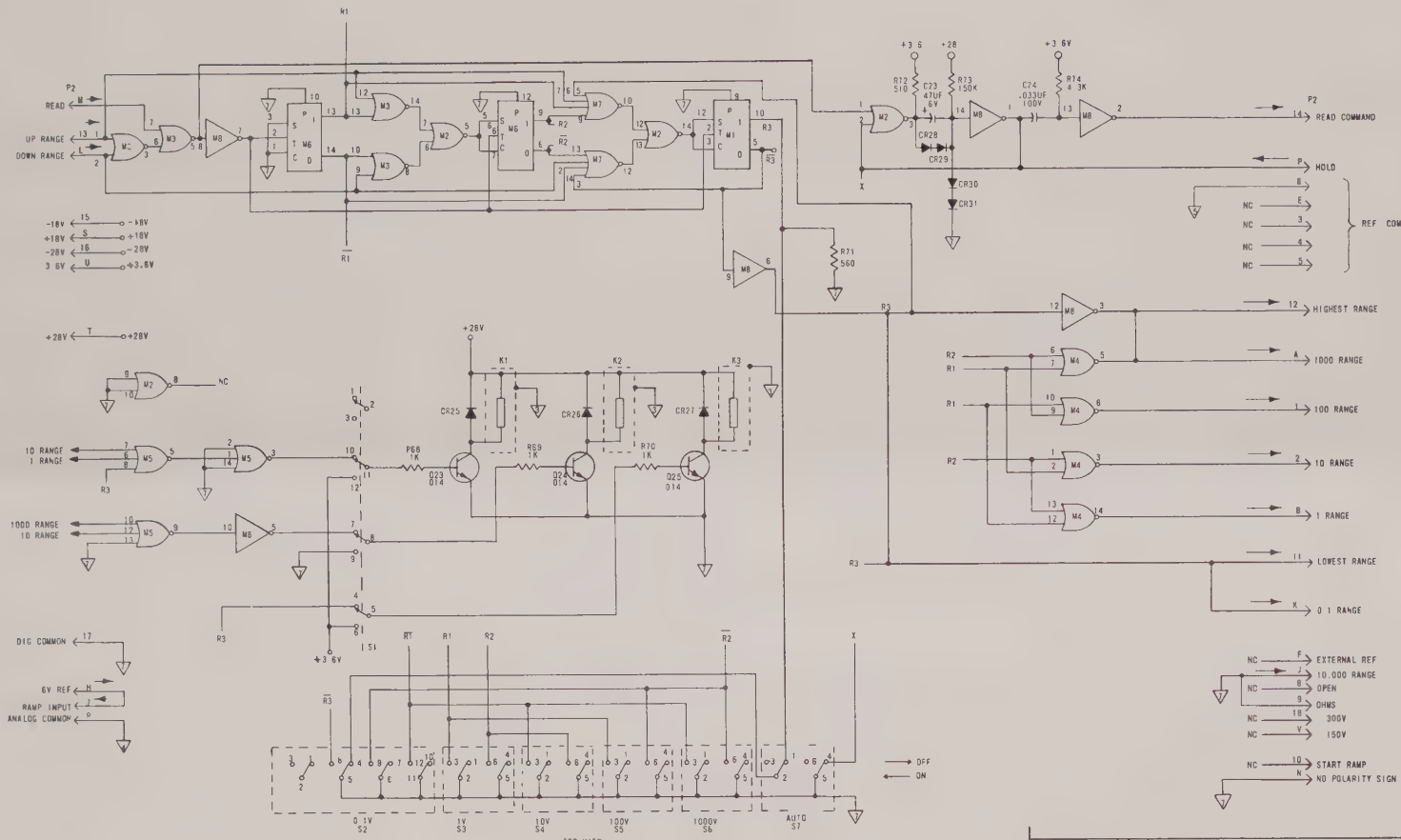
DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN Jim Arteta 5/4/68
CHECK 5/4/68
DESIGN Nau 5/4/68
PROJ ENGR 5/4/68
D Pugs 5/3/68

SCHEMATIC — 212
MILLIVOLT ISOLATOR

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	430708	C

SCALE NONE WT SHEET 1 OF 2



	RANGE LOGIC			RELAY POSITION		
RANGE	R1	R2	R3	k1	k2	k3
0.1V	1	1	1	OPEN	OPEN	OPEN
1V	0	0	0	OPEN	OPEN	CLOSED
10V	1	0	0	OPEN	CLOSED	CLOSED
100V	0	1	0	CLOSED	OPEN	CLOSED
1000V	1	1	0	CLOSED	CLOSED	CLOSED

TABLE A

TOP VIEW S1 & S2

TOP VIEW S3-S7

SEE SHEET 1 OF 2

NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	DANA PART NUMBER	NOMENCLATURE OR DESCRIPTION	CODE IDENT	SPECIFICATION OR VENDOR P/N	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST			

NEXT ASSY	USED ON	REF	REF
	212	NA	FA
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS .XX .030 .XXX .010 ANGLES 0° 30' FORMED ANGLES 1.0

MATERIAL

FINISH

CONTRACT NO.

DANA LABORATORIES INC.
IRVINE, CALIFORNIA

DRAWN Jim Antista 1-22-68
CHECK 5/3/65
DES/GN 5/3/65
PROJ ENGR 5/3/65

SCHEMATIC – 212
MILLIVOLT ISOLATOR

SIZE	CODE IDENT NO	DWG NO.	REV
D	21793	430708	C

SCALE NONE WT | SHEET 2 OF 2

Warranty

It is the practice of Dana Laboratories, Incorporated, to manufacture only products of a quality that will merit customer satisfaction. The company recognizes that customer satisfaction is achieved, not only by delivering products meeting advertised performance specifications and having a high level of reliability, but also by honestly and efficiently fulfilling their warranty obligations as set forth below.

Dana Laboratories, Inc., agrees to correct, either by repair or replacement, any defect of material or workmanship in Dana-manufactured units or components which develop within one year after delivery of the equipment to the original purchaser — provided that the equipment has been subjected only to normal and proper use.

In the event of failure of any component delivered with Dana equipment, but not manufactured by Dana Laboratories, assistance will be given the customer in obtaining, from the original manufacturer, reasonable adjustment under that manufacturer's warranty.

Any item claimed to be defective during the warranty period must be returned to Dana Laboratories, Inc., with transportation charges prepaid. The item will be repaired and returned to the purchaser with return transportation prepaid by Dana unless, of course, the item is found not to be defective or found to be damaged by misuse — in which case it will be returned to the purchaser with repair and transportation billed collect.

DANA

DIALOG

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